IEC 61691-6

Edition 1.0 2009-12

INTERNATIONAL STANDARD

IEEE Std 1076.1™

Behavioural languages –
Part 6: VHDL Analog and Mixed-Signal Extensions

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

PRICE CODE XH

ICS 25.040, 35.060

ISBN 978-0-7381-6283-6

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1076.1 (2007)	93/280/FDIS	93/286/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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IEEE Standard VHDL Analog and Mixed-Signal Extensions

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 17 May 2007

IEEE SA-Standards Board

Abstract: This standard defines the IEEE 1076.1 language, a hardware description language for the description and the simulation of analog, digital, and mixed-signal systems. The language, also informally known as VHDL-AMS, is built on IEEE Std 1076™-2002 (VHDL) and extends it with additions and changes to provide capabilities of writing and simulating analog and mixed-signal models.
Keywords: analog design, computer, computer languages, hardware design, mixed-signal design, VHDL

IEEE introduction

The IEEE 1076.1 language, informally known as VHDL-AMS, is a superset of IEEE Std 1076-2002 (VHDL) that provides capabilities for describing and simulating analog and mixed-signal systems with conservative and nonconservative semantics for the analog portion of the system. The language supports many abstraction levels in electrical and non electrical energy domains. The modeled analog systems arelumped systems that can be described by ordinary differential equations and algebraic equations. The language does not specify any particular technique to solve the equations, but it rather defines the results that must be achieved. The solution of the equations may include discontinuities. Interaction between the digital part of a model and its analog part is supported in a flexible and efficient manner. Finally, support for frequency domain small-signal and noise simulation is provided.

The extension of VHDL to support analog and mixed-signal systems began in 1989, as part of the second revision of IEEE Std 1076 targeted for a 1993 release. A large number of requirements to support analog and mixed-signal systems were submitted, and it soon became apparent that the complexity of the topic required the formation of a separate working group. The design of the IEEE 1076.1 language formally began in 1993, when the IEEE 1076.1 Working Group was formed under the auspices of the Design Automation Standards Committee of the IEEE Computer Society, under Project Authorization Request (PAR) 1076.1. Its charter was to extend the IEEE 1076 (VHDL) language to support the requirements for the description and simulation of analog and mixed-signal systems. The IEEE 1076.1 Working Group approved the draft standard in June 1997. The first release of the draft of IEEE Std 1076.1-1999 was approved by the IEEE Standards Board on 18 March 1999.

The 2007 revision includes changes made to IEEE Std 1076-2002 since the first release of the IEEE 1076.1 standard. It also includes clarification of IEEE 1076.1 language definitions and corrections of typographical errors that were introduced in the 1999 version of the IEEE 1076.1 language reference manual. See the Annex D for a list of changes from the 1999 release.

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BEHAVIOURAL LANGUAGES –

Part 6: VHDL Analog and Mixed-Signal Extensions

0. Overview

This clause describes the purpose, scope, and organization of this standard.

0.1 Purpose and scope

This standard defines IEC 61691-6/IEEE 1076.1™ language, a hardware description language for the description and the simulation of analog, digital, and mixed-signal systems. The language, also informally known as VHDLAMS, is built on the IEC 61691-1-1/IEEE 1076™ (VHDL) language and extends it to provide capabilities of writing and simulating analog and mixed-signal models.

This document contains the complete reference of the IEC 61691-6/IEEE 1076.1 VHDL language, including the unchanged portions of the base language and the extensions. Formally, IEC 61691-6:2009/IEEE Std 1076.1-2007 defines the extensions only, and portions of text marked with change bars are either exclusively part of IEC 61691-6:2009/IEEE Std 1076.1-2007 or define changes compared to IEC 61691-1-1:2004/IEEE Std 1076-2002.[1] Portions of text not marked with change bars are identical in this document and in IEC 61691-1-1:2004/IEEE Std 1076-2002.

The primary audience of this document are implementers of tools supporting the language and advanced users of the language. The document is not intended to provide any introductory or tutorial information. It rather provides formal definitions of language elements and language constructs.

The IEC 61691-6/IEEE 1076.1 language is a superset of the IEC 61691-1-1/IEEE 1076 language (VHDL). As such, any legal IEC 61691-1-1/IEEE 1076 model is a IEC 61691-6/IEEE 1076.1 model, and any IEC 61691-6/IEEE 1076.1 tool shall provide the same simulation results as obtained with an IEC 61691-1-1/IEEE 1076 tool. IEC 61691-1-1:2004/IEEE Std 1076-2002 and IEC 61691-6:2009/IEEE Std 1076.1-2007 will remain separate standards. This means that when IEC 61691-1-1:2004/IEEE Std 1076-2002 is revised, IEC 61691-6:2009/IEEE Std 1076.1-2007 will not be automatically revised accordingly. A separate effort will be required to keep both standards synchronized and to avoid inconsistencies.

0.2 Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in the text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

This standard is dependent upon IEC 61691-1-1:2004/IEEE Std 1076-2002. In addition, certain definitions in this document depend on IEEE Std 1076.2-1996, which describes via standard packages and definitions mathematical functions that can be used within VHDL design units.

IEC 61691-1-1:2004 *Behavioural languages - Part 1-1: VHDL language reference manual*

IEEE Std 1076-2002, *IEEE Standard VHDL Language Reference Manual*.[2, 3, 4]

[1] Information on references can be found in 0.2.

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[4] IEEE Std 1076-2002 was adopted as IEC 61691-1-1:2004.

IEEE Std 1076.2-1996 (Reaff 2002), IEEE Standard VHDL Mathematical Packages.

0.3 Structure and terminology of this standard

This standard is organized into clauses, each of which focuses on some particular area of the language. Within each clause, individual constructs or concepts are discussed in each subclause.

Each subclause describing a specific construct begins with an introductory paragraph. Next, the syntax of the construct is described using one or more grammatical *productions*.

A set of paragraphs describing the meaning and restrictions of the construct in narrative form then follow.

In this document, the word *shall* is used to indicate a mandatory requirement. The word *should* is used to indicate a recommendation. The word *may* is used to indicate a permissible action. The word *can* is used for statements of possibility and capability.

Finally, each clause may end with examples, notes, and references to other pertinent clauses.

0.3.1 Syntactic description

The form of a VHDL description is described by means of context-free syntax using a simple variant of the Backus-Naur Form; in particular:

a) Lowercase words in roman font, some containing embedded underlines, are used to denote syntactic categories, for example:

    formal_port_list

   Whenever the name of a syntactic category is used, apart from the syntax rules themselves, spaces take the place of underlines [thus, “formal port list” would appear in the narrative description when referring to the syntactic category in item a)].

b) Boldface words are used to denote reserved words, for example:

    array

   Reserved words shall be used only in those places indicated by the syntax.

c) A *production* consists of a *left-hand side*, the symbol “::=” (which is read as “can be replaced by”), and a *right-hand side*. The left-hand side of a production is always a syntactic category; the right-hand side is a replacement rule. The meaning of a production is a textual-replacement rule: any occurrence of the left-hand side may be replaced by an instance of the right-hand side.

d) A vertical bar (|) separates alternative items on the right-hand side of a production unless it occurs immediately after an opening brace, in which case it stands for itself, as follows:

    letter_or_digit ::= letter | digit
    choices ::= choice { | choice }

   In the first instance, an occurrence of “letter_or_digit” can be replaced by either “letter” or “digit.” In the second case, “choices” can be replaced by a list of “choice,” separated by vertical bars [see item f) for the meaning of braces].

e) Square brackets [ ] enclose optional items on the right-hand side of a production; thus, the following two productions are equivalent:

    return_statement ::= **return** [expression] ;
    return_statement ::= **return** ; | **return** expression ;

   Note, however, that the initial and terminal square brackets in the right-hand side of the production for signatures (see 2.3.2) are part of the syntax of signatures and do not indicate that the entire right-hand side is optional.