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Digital Test Interchange Format (DTIF)



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Contents

1.	Overview	1
1.1	Scope	1
1.2	Purpose	1
1.3	Application	1
2.	References	2
3.	Definitions and acronyms	2
3.1	Definitions	2
3.2	Acronyms	4
4.	Data organization overview of the DTIF standard environment	4
4.1	UUT Model Group	5
4.2	Stimulus and Response Group	5
4.3	Fault Dictionary Group	5
4.4	Probe Group	5
5.	File specifications	6
5.1	HEADER file	7
5.2	STIMULUS file	9
5.3	PO_RESPONSE file	10
5.4	PI_NAMES file	11
5.5	PO_NAMES file	12
5.6	MAIN_MODEL file	13
5.7	COMPONENT_TYPE file	14
5.8	USER_NODE file	15
5.9	INPUT_PIN_NAMES file	16
5.10	OUTPUT_PIN_NAMES file	17
5.11	NEAR_FROMS_POINTERS file	18
5.12	NEAR_FROMS file	19
5.13	EVENT file	20
5.14	SETTLED_STATE_ONLY file	22
5.15	SETTLED_STATE_&_PULSES file	23
5.16	NODE_SOURCE file	25
5.17	STEPS file	26
5.18	F.D._POPATS file	27
5.19	F.D._FAULT_SIGNATURES file	28
5.20	F.D._PRINT_STRINGS file	30
5.21	TRISTATE_FROMS_POINTERS file	32
5.22	TRISTATE_FROMS file	33
5.23	PSEUDOP_I_NAMES file	34
5.24	TIMING_SETS file	35
5.25	TIMING_PER_PATTERN file	37
5.26	PHASE_CONNECTIONS file	38
5.27	AUXILIARY_PIN_NAMES file	39
5.28	PI_FORMATS file	40
5.29	FORMAT_ATTRIBUTES file	41

5.30 F.D. _CROSS_REFERENCE file	42
5.31 PROBETAG_DEFINITIONS file	43
5.32 PROBETAG_ASSIGNMENTS file	45
5.33 BURSTS file	46
5.34 STIMULUS_TEXT file	47
5.35 NODE_NAMES file	48
5.36 EVENTS_INIT file	49
5.37 EQUIV_FAULTS file	51
5.38 PROBE_DETECTION file	52
5.39 F.D. EQUIV_SETS file	53
6. Conformance	54
6.1 End-to-end test	54
6.2 Diagnostic test using fault dictionary	54
6.3 Diagnostic test using probe	56
Annex A (informative) Implementation overview	59
Annex B (informative) DTIF dependency diagrams	61
Annex C (informative) Example circuit	66
Annex D (informative) IEEE List of Participants	100

Digital Test Interchange Format (DTIF)

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IEEE Standard for Digital Test Interchange Format (DTIF)

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Abstract: The information content and the data formats for the interchange of digital test program data between digital automated test program generators (DATPGs) and automatic test equipment (ATE) for board-level printed circuit assemblies are defined. This information can be broadly grouped into data that defines the following: UUT Model, Stimulus and Response, Fault Dictionary, and Probe.

Keywords: automatic test equipment (ATE), digital automated test program generator (DATPG), digital test interchange format (DTIF), Fault Dictionary data

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IEEE Introduction

[This introduction is not part of IEEE Std 1445-1998, IEEE Standard for Digital Test Interchange Format (DTIF).]

A digital automated test program generator (DATPG) produces test pattern and diagnostic data that can be used for testing printed circuit assemblies on automatic test equipment (ATE). The use of several DATPGs, all with individual output formats, created a need for many unique post-processors to be developed and maintained for the life of the ATE. These post-processors supported the link from specific DATPGs to specific testers. The proliferation of unique formats and post-processors created logistical support problems and therefore identified a need for standardization. A DATPG and ATE independent output data format is required to limit the number of post-processors (one for each ATE) requiring life cycle support. The digital test interchange format (DTIF) was chosen because of its wide use and because it was becoming known in industry as the de facto standard.

This document provides the basis to standardize digital test information for use on ATE. The digital test information consists of the unit under test (UUT) Model information, Stimulus and Response data, Fault Dictionary data, and Probe data.

DTIF is unique from other standards such as IEEE P1450 (Draft 0.95, dated July 1998),¹ Draft Standard Test Interface Language (STIL) for Digital Test Vector Data, and IEEE Std 1029.1-1991, IEEE Standard for Waveform and Vector Exchange Specification (WAVES). STIL is being developed to standardize the output interface of existing computer-aided engineering (CAE) tools with the input interface of ATE for integrated circuit (IC) testing only. WAVES is a hardware descriptive language used for defining stimulus and response, and their associated timing for IC/board-level design. Neither STIL nor WAVES provides for board-level fault diagnostics.

A future revision of this standard will consider the use of the information model.

¹ IEEE P1450 is an IEEE authorized standards project that was not approved by the IEEE-SA Standards Board at the time this publication went to press. For information about obtaining the draft, contact the IEEE.

Digital Test Interchange Format (DTIF)

1. Overview

The digital test interchange format (DTIF) is designed to provide a mechanism for digital test data interchange independent of specific digital automated test program generators (DATPGs) and test systems. The DTIF provides a neutral database for the development and delivery of digital simulation based test program sets (TPSs). DTIF functionally supports the unit under test (UUT) Model, Stimulus and Response, Fault Dictionary, and Probe databases.

1.1 Scope

This standard defines the information content and the data formats for the interchange of digital test program data between DATPGs and automatic test equipment (ATE) for board-level printed circuit assemblies. This information can be broadly grouped into data that defines the following:

- a) UUT Model;
- b) Stimulus and Response;
- c) Fault Dictionary;
- d) Probe.

1.2 Purpose

The purpose of this standard is to provide a standard output format for test data generated by a DATPG. A DATPG produces test patterns and fault diagnostic data for ATE. This data is used in applications such as board-level assemblies where diagnostic data interchange is important.

1.3 Application

This standard is primarily intended for use by digital simulator developers/maintainers and TPS developers/maintainers.

2. References

This standard shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply.

ANSI X3.4-1986 (Reaff 1997), Information Systems—Coded Character Sets—7-Bit American National Standard Code for Information Interchange (7-Bit ASCII).¹

IEEE Std 100-1996, IEEE Standard Dictionary of Electrical and Electronics Terms.²

3. Definitions and acronyms

3.1 Definitions

The following definitions are for use with this standard. For other uses and for definitions not contained herein, see IEEE Std 100-1996. Unless otherwise indicated, the ATPG subcommittee formulated all terms defined in this subclause.

3.1.1 burst: A set of stimulus patterns and related unit under test (UUT) responses that are set up, applied, and read as a group. A test program may employ more than one burst to provide the stimuli and responses necessary to test the UUT.

3.1.2 channel: The tester electronics associated with a digital input/output (I/O) pin that either drives or senses a particular node on the unit under test (UUT).

3.1.3 circuit simulator: A software program that predicts a circuit's response to a given stimulus.

3.1.4 digital automatic test program generator (DATPG): A program, often based on simulation, that aids in the development of test patterns and diagnostic information from the model of a unit under test (UUT).

3.1.5 dynamic patterns: A set of controlled, time-variant patterns within a time interval.

3.1.6 edge: A logic state transition that is considered instantaneous for a given pattern in the simulation process.

3.1.7 end-to-end test: A test sequence to establish pass (functioning properly) or fail (not functioning properly) conditions. *Syn:* **go/nogo test.**

3.1.8 fault set: A group of one or more faults with the same fault signature.

3.1.9 fault signature: A set of unique primary output patterns in which the fault will produce a response different from the good machine response.

3.1.10 fault title: A two-part description that includes a node name and a fault type [i.e., <U5>6 SA1 (component: U5, pin: 6, fault type: Stuck at 1)].

3.1.11 go/nogo test: *See:* **end-to-end test.**

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