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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Semiconductor devices – Hot carrier test on MOS transistors

Dispositifs à semiconducteurs – Essai de porteur chaud sur les transistors MOS

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland
Email: inmail@iec.ch
Web: www.iec.ch

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Tél.: +41 22 919 02 11
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CONTENTS

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FOREWORD

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The text of this standard is based on the following documents:

FDIS	Report on voting
47/2041/FDIS	47/2048/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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- withdrawn,
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES – HOT CARRIER TEST ON MOS TRANSISTORS

1 Scope

This standard describes the wafer level hot carrier test on NMOS and PMOS transistors. The test is intended to determine whether the single transistors in a certain (C)MOS process meet the required hot carrier lifetime.

2 Abbreviations and letter symbols

In this document the following abbreviations and letter symbols apply:

MOS	Metal Oxide Semiconductor
NMOS	n-channel MOS transistor
PMOS	p-channel MOS transistor
(C)MOS	Complementary MOS
L [µm]	length of polysilicon gate of MOS transistor
W [µm]	width of polysilicon gate of MOS transistor
$L_{nominal}$ [µm]	minimum L allowed by the design rules of the process
$W_{nominal}$ [µm]	minimum W allowed by the design rules of the process
V_{gs} [V]	gate-source voltage of MOS transistor
V_{ds} [V]	drain-source voltage of MOS transistor
V_{bs} [V]	backgate-source voltage of MOS transistor
I_{ds} [µA]:	drain-source current of MOS transistor
I_b [µA]	substrate current of MOS transistor
I_g [nA]	gate current of MOS transistor
$V_{gs,stress}$ [V]	V_{gs} biasing condition during hot carrier stress
$V_{ds,stress}$ [V]	V_{ds} biasing condition during hot carrier stress
V_{ds,use_max} [V]	maximum V_{ds} allowed by the design rules of the process as stated in the design manual
$V_{ds,breakdown}$ [V]	V_{ds} at which avalanche or punch-through currents become dominant; defined as V_{ds} at which I_{ds}= 1,5 × (I_{ds} at V_{ds,use_max}) while V_{gs}= V_{ds,use_max}
V_t [V]	threshold voltage of MOS transistor defined as V_{gs} voltage at which I_{ds}= 0,01 × W / L [µA]. Other (commonly agreed) definitions of V_t are also allowed as long as this is clearly reported.
g_m [µA/V]	transconductance of MOS transistor
$g_{m,max}$ [µA/V]	maximum transconductance of MOS transistor
$I_{ds,sat}$ [µA]	saturated drain-source current at V_{gs}= V_{ds}= $V_{ds,use\_,max}$; $I_{ds,sat\_forward}$ measured with source and drain having same polarity as during stress, $I_{ds,sat\_reverse}$ measured with source and drain polarity interchanged with respect to stress.
L(MOST)	length of the square MOS transistor (L = W)
$g_{m,max}$ (MOST)	$g_{m,max}$ of the square MOS transistor (L = W)