

**Device embedding assembly technology - Part 2-5:  
Guidelines - Implementation of a 3D data format for  
device embedded substrate**

**EESTI STANDARDI EESSÕNA****NATIONAL FOREWORD**

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ICS 31.180, 31.190

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ICS 31.180; 31.190

English Version

**Device embedding assembly technology - Part 2-5: Guidelines -  
Implementation of a 3D data format for device embedded  
substrate  
(IEC 62878-2-5:2019)**

Techniques d'assemblage avec intégration d'appareils -  
Partie 2-5 : Lignes directrices - Mise en œuvre d'un format  
de données 3D pour un substrat avec appareils intégrés  
(IEC 62878-2-5:2019)

Montageverfahren für eingebettete Bauteile - Teil 2-5:  
Implementierung eines 3D-Datenformats für Trägermaterial  
mit eingebetteten Bauteilen  
(IEC 62878-2-5:2019)

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European Committee for Electrotechnical Standardization  
Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

**CEN-CENELEC Management Centre: Rue de la Science 23, B-1040 Brussels**

## European foreword

The text of document 91/1557/CDV, future edition 1 of IEC 62878-2-5, prepared by IEC/TC 91 "Electronics assembly technology" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 62878-2-5:2019.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2020-07-21
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2022-10-21

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The text of the International Standard IEC 62878-2-5:2019 was approved by CENELEC as a European Standard without any modification.

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**DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –****Part 2-5: Guidelines – Implementation of a 3D data format  
for device embedded substrate**

## FOREWORD

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International Standard IEC 62878-2-5 has been prepared by IEC technical committee 91: Electronics assembly technology.

This first edition cancels and replaces IEC PAS 62878-2-5 published in 2015. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) the title has been changed to "Implementation of a 3D data format for device embedded substrate" from "Requirements of design data format for device embedded substrate";
- b) the scope of this implementation has changed to not include SiPs.

The text of this International Standard is based on the following documents:

CDV	Report on voting
91/1557/CDV	91/1589/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

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- replaced by a revised edition, or
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## DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

### Part 2-5: Guidelines – Implementation of a 3D data format for device embedded substrate

#### 1 Scope

This part of IEC 62878 specifies requirements based on XML schema that represents a design data format for device embedded substrate, which is a board comprising embedded active and passive devices whose electrical connections are made by means of a via, electroplating, conductive paste or printing of conductive material.

This data format is to be used for simulation (e.g. stress, thermal, EMC), tooling, manufacturing, assembly, and inspection requirements. Furthermore, the data format is used for transferring information among printed board designers, printed board simulation engineer, manufacturers, and assemblers.

This part of IEC 62878 applies to substrates using organic material. It neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as M-type business model in IEC 62421.

#### 2 Normative references

There are no normative references in this document.

#### 3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

##### 3.1

##### **artwork information**

information that shows a SiP not included in net and figure data in board (symbol mark, inside of SiP, mould, spacer, remarks, etc.)

##### 3.2

##### **board information**

total information of a device-embedded substrate, including embedded devices

##### 3.3

##### **chip stack**

package of semiconductor chips stacked vertically

##### 3.4

##### **clearance**

area around a through-hole where there is no conductor to prevent electrical connection between a large conductor area, such as that of a power supply or a ground and a plated through-hole