EMC IC modelling - Part 6: Models of integrated circuits for pulse immunity behavioural simulation - Conducted pulse immunity modelling (ICIM-CPI)

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NATIONAL FOREWORD

See Eesti standard EVS-EN IEC 62433-6:2020 sisaldab Euroopa standardi EN IEC 62433-6:2020 ingliskeelset teksti.	This Estonian standard EVS-EN IEC 62433-6:2020 consists of the English text of the European standard EN IEC 62433-6:2020.
Standard on jõustunud sellekohase teate avaldamisega EVS Teatajas	This standard has been endorsed with a notification published in the official bulletin of the Estonian Centre for Standardisation.
Euroopa standardimisorganisatsioonid on teinud Euroopa standardi rahvuslikele liikmetele kättesaadavaks 06.11.2020.	Date of Availability of the European standard is 06.11.2020.
Standard on kättesaadav Eesti Standardikeskusest.	The standard is available from the Estonian Centre for Standardisation.

Tagasisidet standardi sisu kohta on võimalik edastada, kasutades EVS-i veebilehel asuvat tagasiside vormi või saates e-kirja meiliaadressile standardiosakond@evs.ee.

ICS 31.200

EUROPEAN STANDARD

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EN IEC 62433-6

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EMC IC modelling - Part 6: Models of integrated circuits for Pulse immunity behavioural simulation - Conducted Pulse Immunity (ICIM-CPI) (IEC 62433-6:2020)

Modèles de circuits intégrés pour la CEM - Partie 6: Modèles de circuits intégrés pour la simulation du comportement d'immunité aux impulsions - Modélisation de l'immunité aux impulsions conduites (ICIM-CPI) (IEC 62433-6:2020)

EMV-IC-Modellierung - Teil 6: Modelle integrierter Schaltungen für die Simulation des Verhaltens bei Störfestigkeit gegen Impulse - Modellierung der Störfestigkeit gegen leitungsgeführte Impulse (ICIM-CPI) (IEC 62433-6:2020)

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Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Ref. No. EN IEC 62433-6:2020 E

European foreword

The text of document 47A/1090/CDV, future edition 1 of IEC 62433-6, prepared by SC 47A "Integrated circuits" of IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 62433-6:2020.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2021-07-27
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2023-10-27

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In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 62433-2:2017	NOTE	Harmonized as EN 62433-2:2017 (not modified)
CISPR 16-1-4:2019	NOTE	Harmonized as EN IEC 55016-1-4:2019 (not modified)
CISPR 17	NOTE	Harmonized as EN 55017

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

Publication	Year	Title	EN/HD	Year
IEC 61000-4-2	-	Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test	EN 61000-4-2	-
IEC 61000-4-4	-	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test	EN 61000-4-4	-
IEC 62215-3	-	Integrated circuits - Measurement of impulse immunity - Part 3: Non-synchronous transient injection method	EN 62215-3	-
IEC 62433-1	-	EMC IC modelling - Part 1: General modelling framework	EN IEC 62433-1	-
IEC 62433-4	-	EMC IC modelling - Part 4: Models of integrated circuits for RF immunity behavioural simulation - Conducted immunity modelling (ICIM-CI)	EN 62433-4	-
IEC 62615	-	Electrostatic discharge sensitivity testing - Transmission line pulse (TLP) - Component level	-	-

IEC 62433-6

Edition 1.0 2020-09

INTERNATIONAL STANDARD

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colour inside

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Modèles de circuits intégrés pour la CEM –
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IEC 62433-6:2020-09(en-fr)

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IEC 62433-6

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INTERNATIONAL STANDARD

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CONTENTS

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EMC IC MODELLING –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 62433-6 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

CDV	Report on voting
47A/1090/CDV	47A/1098/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62433 series, published under the general title *EMC IC modelling*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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EMC IC MODELLING –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

1 Scope

The objective of this part of IEC 62433 is to describe the extraction flow for deriving an immunity macro-model of an Integrated Circuit (IC) against conducted Electrostatic Discharge (ESD) according to IEC 61000-4-2 and Electrical Fast Transients (EFT) according to IEC 61000-4-4.

The model addresses physical damages due to overvoltage, thermal damage and other failure modes. Functional failures can also be addressed.

This model allows the immunity simulation of the IC in an application. This model is commonly called "Integrated Circuit Immunity Model Conducted Pulse Immunity", ICIM-CPI.

The described approach is suitable for modelling analogue, digital and mixed-signal ICs. Several terminals of an IC can be part of a single model (e.g. input, output and supply pins). The implementation of the model is capable of representing the non-linear behaviour of overvoltage protection circuits.

The model can be implemented for the use in different software tools for circuit simulation in time-domain. The described modelling approach allows simulating device failure due to ESD or EFT at component and system level considering all components necessary for the immunity simulation of an IC, such as a PCB or external protection elements.

This document demonstrates, in detail, the construction of models in a defined XML-based format which is suitable for the exchange of models without any deeper knowledge of the semiconductor circuit. However, the model functionality can be implemented in different formats including, but not limited to, tables, SPICE[1] [1] netlists, hardware description languages such as VHDL-AMS [2] and Verilog-AMS [3].

This document provides:

- the description of ICIM-CPI macro-model elements representing electrical, thermal or logical behaviour of the IC.
- a universal data exchange format based on XML.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61000-4-2, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*

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1 Numbers in square brackets refer to the bibliography.