

EMC IC modelling - Part 6: Models of integrated circuits
for pulse immunity behavioural simulation - Conducted
pulse immunity modelling (ICIM-CPI)

EESTI STANDARDI EESSÕNA

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See Eesti standard EVS-EN IEC 62433-6:2020 sisaldab Euroopa standardi EN IEC 62433-6:2020 ingliskeelset teksti.	This Estonian standard EVS-EN IEC 62433-6:2020 consists of the English text of the European standard EN IEC 62433-6:2020.
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English Version

EMC IC modelling - Part 6: Models of integrated circuits for
Pulse immunity behavioural simulation - Conducted Pulse
Immunity (ICIM-CPI)
(IEC 62433-6:2020)

Modèles de circuits intégrés pour la CEM - Partie 6:
Modèles de circuits intégrés pour la simulation du
comportement d'immunité aux impulsions - Modélisation de
l'immunité aux impulsions conduites (ICIM-CPI)
(IEC 62433-6:2020)

EMV-IC-Modellierung - Teil 6: Modelle integrierter
Schaltungen für die Simulation des Verhaltens bei
Störfestigkeit gegen Impulse - Modellierung der
Störfestigkeit gegen leitungsgeführte Impulse (ICIM-CPI)
(IEC 62433-6:2020)

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European foreword

The text of document 47A/1090/CDV, future edition 1 of IEC 62433-6, prepared by SC 47A "Integrated circuits" of IEC/TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 62433-6:2020.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2021-07-27
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IEC 62433-2:2017	NOTE	Harmonized as EN 62433-2:2017 (not modified)
CISPR 16-1-4:2019	NOTE	Harmonized as EN IEC 55016-1-4:2019 (not modified)
CISPR 17	NOTE	Harmonized as EN 55017

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

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NOTE 1 Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: www.cenelec.eu.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 61000-4-2	-	Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test	EN 61000-4-2	-
IEC 61000-4-4	-	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test	EN 61000-4-4	-
IEC 62215-3	-	Integrated circuits - Measurement of impulse immunity - Part 3: Non-synchronous transient injection method	EN 62215-3	-
IEC 62433-1	-	EMC IC modelling - Part 1: General modelling framework	EN IEC 62433-1	-
IEC 62433-4	-	EMC IC modelling - Part 4: Models of integrated circuits for RF immunity behavioural simulation - Conducted immunity modelling (ICIM-CI)	EN 62433-4	-
IEC 62615	-	Electrostatic discharge sensitivity testing - Transmission line pulse (TLP) - Component level	-	-

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EMC IC modelling –

**Part 6: Models of integrated circuits for pulse immunity behavioural simulation –
Conducted pulse immunity modelling (ICIM-CPI)**

Modèles de circuits intégrés pour la CEM –

**Partie 6: Modèles de circuits intégrés pour la simulation du comportement
d'immunité aux impulsions – Modélisation de l'immunité aux impulsions
conduites (ICIM-CPI)**



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INTERNATIONAL STANDARD

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EMC IC modelling –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

Modèles de circuits intégrés pour la CEM –

Partie 6: Modèles de circuits intégrés pour la simulation du comportement d'immunité aux impulsions – Modélisation de l'immunité aux impulsions conduites (ICIM-CPI)

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CONTENTS

FOREWORD	5
1 Scope	7
2 Normative references	7
3 Terms, definitions, abbreviated terms and conventions	8
3.1 Terms and definitions	8
3.2 Abbreviated terms	11
3.3 Conventions	11
4 Philosophy	11
5 ICIM-CPI model structure	12
5.1 General	12
5.2 PPN	14
5.2.1 Typical structure of a PPN	14
5.2.2 PDN description	15
5.2.3 NLB description	16
5.3 FB description	16
6 CPIML format	18
6.1 General	18
6.2 CPIML structure	19
6.3 Global elements	20
6.4 Header section	20
6.5 Lead_definitions section	20
6.6 Macromodels section	21
6.7 Validity section	22
6.8 PDN	22
6.9 NLB	22
6.9.1 General	22
6.9.2 Attribute definitions	23
6.9.3 Data description	24
6.10 FB	25
6.10.1 General	25
6.10.2 Attribute definitions	26
6.10.3 Data description	30
Annex A (informative) Extraction of model components	34
A.1 General	34
A.2 PPN description	34
A.3 PDN Extraction	34
A.3.1 General	34
A.3.2 S/Z/Y-parameter measurement	34
A.3.3 Conventional one-port method	35
A.3.4 Two-port method for low impedance measurement	35
A.3.5 Two-port method for high impedance measurement	36
A.4 NLB extraction	36
A.4.1 General	36
A.4.2 TLP test method	37
A.5 FB extraction	39
A.5.1 General	39

A.5.2	Example of FB data in case of test criteria type = Class E_IC	39
A.5.3	Example of FB data in case of test criteria type = Class C_IC	41
Annex B (informative)	NLB implementation techniques in a circuit simulator	42
B.1	General.....	42
B.2	NLB modelling based on a R/I table	42
B.3	NLB modelling based on a switch based model	42
B.4	NLB modelling based on physical device model	43
Annex C (informative)	Example of ICIM-CPI model	45
C.1	General.....	45
C.2	Example of Power switch ICIM-CPI model.....	45
C.2.1	General	45
C.2.2	CPI model.....	45
C.2.3	ICIM-CPI model use	48
C.3	Example of 32-bit microcontroller ICIM-CPI model	50
C.3.1	General	50
C.3.2	CPI model.....	51
Bibliography.....		54
Figure 1	– Structure of the ICIM-CPI model.....	13
Figure 2	– Example of an ICIM-CPI model of an electronic board.....	14
Figure 3	– Structure of a typical PPN	15
Figure 4	– Characteristics of a voltage pulse entering the DI during a TLP test	17
Figure 5	– Example of defect monitored at the OO when a disturbance is applied to the DI.....	18
Figure 6	– CPIML inheritance hierarchy	19
Figure 7	– Example of a NLB external file	25
Figure 8	– Example of an external FB file	33
Figure A.1	– Conventional one-port S-parameters measurement.....	35
Figure A.2	– Two-port method for low impedance measurement	35
Figure A.3	– Two-port method for high impedance measurement	36
Figure A.4	– Example of I/V measurements to extract NLB	37
Figure A.5	– TLP method set-up (not powered IC)	38
Figure A.6	– Example of NLB extraction using standard TLP pulse	38
Figure A.7	– Graphs for identification of IC failure mechanism for destruction prediction.....	40
Figure B.1	– NLB model based on a R/I table.....	42
Figure B.2	– Example of a generic model architecture based on switches for NLB behavioural modelling	43
Figure B.3	– Example of core MOS large signal model of the GGNMOS	43
Figure C.1	– Use of the ICIM-CPI model for simulation	45
Figure C.2	– Power switch V/I curve for 50 ns-pulse width	46
Figure C.3	– Power switch ICIM-CPI model.....	46
Figure C.4	– Power switch ICIM-CPI model use for ESD protection design	49
Figure C.5	– Calculated voltage at Power switch pin for different ESD protection capacitor values.....	49
Figure C.6	– Voltage at Power switch pin for fog lamp left and right sides.....	50
Figure C.7	– Example of 32-bit microcontroller protection devices	50

Table 1 – Attributes of <i>Lead</i> tag in the <i>Lead_definitions</i> section	20
Table 2 – Compatibility between the <i>Mode</i> and <i>Type</i> fields for correct CPIML annotation.....	21
Table 3 – Definition of the <i>Lead</i> tag for <i>Nlb</i> section	22
Table 4 – Default values of <i>Unit_voltage</i> and <i>Unit_current</i>	24
Table 5 – Allowed file extensions for <i>Data_files</i>	24
Table 6 – Definition of the <i>Lead</i> tag in <i>Fb</i> section	26
Table 7 – <i>Table</i> sub-attributes definition	27
Table 8 – <i>Pulse_characteristics</i> parameters definition	27
Table 9 – <i>Test_criteria</i> parameters definition	28
Table A.1 – Example of FB data corresponding to Class E _{IC} failure.....	41
Table A.2 – Example of FB data corresponding to Class C _{IC} failure	41
Table C.1 – Synthesis Peak voltage and Energy for different pulse widths	46

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EMC IC MODELLING –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

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The text of this International Standard is based on the following documents:

CDV	Report on voting
47A/1090/CDV	47A/1098/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62433 series, published under the general title *EMC IC modelling*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

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EMC IC MODELLING –

Part 6: Models of integrated circuits for pulse immunity behavioural simulation – Conducted pulse immunity modelling (ICIM-CPI)

1 Scope

The objective of this part of IEC 62433 is to describe the extraction flow for deriving an immunity macro-model of an Integrated Circuit (IC) against conducted Electrostatic Discharge (ESD) according to IEC 61000-4-2 and Electrical Fast Transients (EFT) according to IEC 61000-4-4.

The model addresses physical damages due to overvoltage, thermal damage and other failure modes. Functional failures can also be addressed.

This model allows the immunity simulation of the IC in an application. This model is commonly called "Integrated Circuit Immunity Model Conducted Pulse Immunity", ICIM-CPI.

The described approach is suitable for modelling analogue, digital and mixed-signal ICs. Several terminals of an IC can be part of a single model (e.g. input, output and supply pins). The implementation of the model is capable of representing the non-linear behaviour of overvoltage protection circuits.

The model can be implemented for the use in different software tools for circuit simulation in time-domain. The described modelling approach allows simulating device failure due to ESD or EFT at component and system level considering all components necessary for the immunity simulation of an IC, such as a PCB or external protection elements.

This document demonstrates, in detail, the construction of models in a defined XML-based format which is suitable for the exchange of models without any deeper knowledge of the semiconductor circuit. However, the model functionality can be implemented in different formats including, but not limited to, tables, SPICE[1] 1 netlists, hardware description languages such as VHDL-AMS [2] and Verilog-AMS [3].

This document provides:

- the description of ICIM-CPI macro-model elements representing electrical, thermal or logical behaviour of the IC.
- a universal data exchange format based on XML.

2 Normative references

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IEC 61000-4-2, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*

¹ Numbers in square brackets refer to the bibliography.