

INTERNATIONAL STANDARD

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Test methods for electrical materials, printed boards and other interconnection structures and assemblies –

Part 5-501: General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes

Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles –

Partie 5-501: Méthodes d'essai générales pour les matériaux et les ensembles – Essais de résistance d'isolement en surface (RIS) des flux de brasage



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INTERNATIONAL
ELECTROTECHNICAL
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COMMISSION
ELECTROTECHNIQUE
INTERNATIONALE

ICS 31.180

ISBN 978-2-8322-9289-1

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CONTENTS

FOREWORD.....	4
1 Scope.....	6
2 Normative references	6
3 Terms and definitions	7
4 Equipment/Apparatus	7
4.1 Measurement instrument.....	7
4.2 Resistor verification coupon	8
4.3 Damp heat chamber.....	8
4.4 Additional apparatus	9
4.4.1 Ionic contamination test system	9
4.4.2 Drying oven	9
4.4.3 Camera	9
4.4.4 Backlight panel	9
5 Test coupons.....	9
5.1 General.....	9
5.2 IEC TB144 (IPC B53) test coupon	9
5.3 Laminate.....	10
5.4 Coupons for testing.....	10
5.5 Chamber controls.....	10
5.6 Blank process controls	11
5.7 Test conditions	11
5.7.1 Fluxes not intended for cleaning	11
5.7.2 Fluxes intended for cleaning	11
5.8 Test duration.....	11
5.9 Test voltage	11
5.10 Connecting the test coupons	11
5.10.1 General	11
5.10.2 Connector/test rack	11
5.10.3 Direct wiring	12
5.11 Cable connection	12
5.12 Coupon orientation in the chamber	12
6 Coupon preparation	13
6.1 General.....	13
6.2 Coupon cleaning	13
6.3 Identification	13
6.4 Inspection	13
6.5 Storage.....	13
6.6 No clean fluxes	14
6.7 Cleanable type fluxes.....	14
6.8 Solder paste coupons	14
6.8.1 Coupon preparation	14
6.8.2 Cleaning of coupons	15
6.9 Preparation of coupons for chamber	15
7 Test procedure	15
8 Measurements.....	15
9 Evaluation	15

10 Reporting.....	16
Annex A (informative) General advice for testing	17
A.1 Test coupons	17
A.2 Test coupon development	17
A.3 Sampling.....	17
A.3.1 General	17
A.3.2 Coupon count	17
A.3.3 Sample sizes	17
A.3.4 Characterising materials	17
A.3.5 Characterising process(es)	17
A.3.6 Derived unit of SIR	17
A.3.7 Set-up parameters	18
A.4 Humidity	18
A.5 Voltage	18
Bibliography.....	19
Figure 1 – SIR pattern	6
Figure 2 – Example of a resistor verification coupon	8
Figure 3 – IPC B53 Surface insulation resistance pattern.....	10
Figure 4 – Connector arrangement.....	12
Figure 5 – Specimen orientation in test chamber.....	12
Figure 6 – Coupon orientation in test chamber.....	13
Table 1 – Coupons for surface insulation resistance (SIR) testing.....	14

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS
AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –****Part 5-501: General test methods for materials and assemblies –
Surface insulation resistance (SIR) testing of solder fluxes**

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IEC 61189-5-501 has been prepared by IEC technical committee 91: Electronics assembly technology. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1645/CDV	91/1672/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, printed boards and other interconnection structures and assemblies*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

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TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 5-501: General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes

1 Scope

This part of IEC 61189 is used to quantify the deleterious effects of flux residues on surface insulation resistance (SIR) in the presence of moisture.

Interdigitated comb patterns comprising long parallel electrodes on an IPC B53 standardized test coupon are used for the evaluation. Coupons are conditioned and measurements taken at a high temperature and humidity. The electrodes are electrically biased during conditioning to facilitate electrochemical reactions, as shown in Figure 1 and Figure 3.

Reference can be made to IEC TR 61189-5-506, which examines different geometry comb patterns: 400 μm x 500 μm ; 400 μm x 200 μm ; and 318 μm x 318 μm .

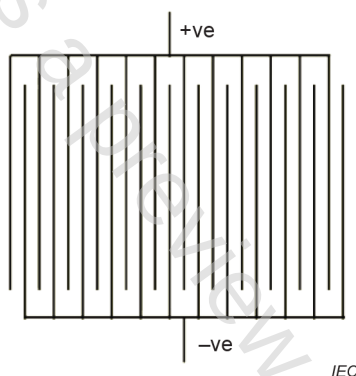


Figure 1 – SIR pattern

Specifically, this method is designed to simultaneously assess:

- leakage current caused by ionized water films and electrochemical degradation of test vehicle, (corrosion, dendritic growth);
- provide metrics that can appropriately be used for binary classification (e.g. go/no go; pass/fail);
- compare, rank or characterize materials and processes.

This test is carried out at high humidity and heat conditions.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-1:2013, *Environmental testing – Part 1: General and guidance*

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60068-2-67, *Environmental testing – Part 2-67: Tests – Test Cy: Damp heat, steady state, accelerated test primarily intended for components*

IEC 60068-2-78, *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*

IEC 60194-2, *Printed boards design, manufacture and assembly – Vocabulary – Part 2: Common usage in electronic technologies as well as printed board and electronic assembly technologies*

IEC 61189-5-504, *Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 5-504: General test methods for materials and assemblies – Process ionic contamination testing (PICT)*

IEC TR 61189-5-506, *Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 5-506: General test methods for materials and assemblies – An intercomparison evaluation to implement the use of fine pitch test structures for surface insulation resistance (SIR) testing of solder fluxes in accordance with IEC 61189-5-501*

IEC 61190-1-3, *Attachment materials for electronic assembly – Part 1-3: Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solder for electronic soldering applications*

IEC 61249-2-7, *Materials for printed boards and other interconnecting structures – Part 2-7: Reinforced base materials clad and unclad – Epoxide woven E-glass laminated sheet of defined flammability (vertical burning test), copper-clad*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60068-1, IEC 60068-2-58, IEC 60194-2, and IEC 61190-1-3 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

4 Equipment/Apparatus

4.1 Measurement instrument

This shall consist of a measuring device capable of measuring insulation resistance in the range of at least $10^6 \Omega$ to $10^{12} \Omega$.

It shall be capable of measuring and recording each individual test channel/pattern. The measurement circuit shall incorporate a 1 M Ω current limiting resistor in each current pathway.

The tolerance of the total measurement system shall be

- $\pm 5 \%$ up to $10^{10} \Omega$ at 5 V;
- $\pm 10 \%$ between $10^{10} \Omega$ to $10^{11} \Omega$ at 5 V;
- $\pm 20 \%$ above $10^{11} \Omega$ at 5 V.

If a different test voltage is to be used, the measurement circuit shall be assessed at that voltage rather than the 5 V stipulated. See Clause A.5 for additional information on test voltages.

The resistors used to confirm the 'total measurement system tolerance' defined above, shall have a purchased tolerance of

- $\pm 0,1 \%$ up to and including $10^6 \Omega$;
- $\pm 1 \%$ above $10^6 \Omega$ and up to and including $10^8 \Omega$;
- $\pm 5 \%$ above $10^8 \Omega$ and up to and including $10^{10} \Omega$;
- $\pm 10 \%$ above $10^{10} \Omega$.