

INTERNATIONAL STANDARD

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**Semiconductor devices – Reliability test method for silicon carbide discrete metal-oxide semiconductor field effect transistors –
Part 1: Test method for bias temperature instability**

Dispositifs à semiconducteurs – Méthode d'essai de fiabilité pour les transistors à effet de champ métal-oxyde-semiconducteurs discrets en carbure de silicium –

Partie 1: Méthode d'essai pour la mesure de la dérive de la tension de seuil après polarisation électrique en température



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**SEMICONDUCTOR DEVICES –
RELIABILITY TEST METHOD FOR SILICON CARBIDE DISCRETE
METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS –****Part 1: Test method for bias temperature instability****FOREWORD**

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Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

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INTRODUCTION

One reliability issue for silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) is gate-source threshold voltage shift under gate-source voltage stress. Gate-source threshold voltage is a key parameter to represent switching characteristics of MOSFETs. Since the shift value tends to be larger than that of conventional Si based devices, it is indispensable to establish an International Standard with regard to evaluation of gate-source threshold voltage shift as a reliability issue.

This document defines the evaluation method of gate-source threshold voltage shift under continuous temperature and gate-source voltage stress on SiC MOSFETs.

SEMICONDUCTOR DEVICES – RELIABILITY TEST METHOD FOR SILICON CARBIDE DISCRETE METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS –

Part 1: Test method for bias temperature instability

1 Scope

This part of IEC 63275 gives a test method to evaluate gate threshold voltage shift of silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) using room temperature readout after applying continuous positive gate-source voltage stress at elevated temperature. The proposed method accepts a certain amount of recovery by allowing large delay times between stress and measurement (up to 10 h).

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-8, *Semiconductor devices – Discrete devices – Part 8: Field-effect transistors*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60747-8 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
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4 Requirements

4.1 Sample

Unless otherwise specified, a minimum of four samples is recommended for each test condition to evaluate representative behaviour of $V_{GS(th)}$ drift. When the test method is applied to qualify reliability of product, the sample size should be defined by taking into consideration device-to-device deviation of shift value of $V_{GS(th)}$ and target application of the product.

4.2 Test temperature

The test is performed at the temperature within the maximum rating of the sample.

4.3 Test voltage

The test is performed at the V_{GS} within the maximum rating of the sample. The tests in this document treat only positive V_{GS} stress.