Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)

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EUROPEAN STANDARD

NORME EUROPÉENNE

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English Version

Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM) (IEC 60749-26:2013)

Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques - Partie 26: Essai de sensibilité aux décharges électrostatiques (DES) - Modèle du corps humain (HBM)
(CEI 60749-26:2013)

Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 26: Prüfung der Empfindlichkeit gegen elektrostatische Entladungen (ESD) - Human Body Model (HBM)
(IEC 60749-26:2013)

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Ref. No. EN 60749-26:2014 E

Foreword

This document (EN 60749-26:2014) consists of the text of IEC 60749-26:2013 prepared by IEC/TC 47 "Semiconductor devices", in collaboration with Technical Committee 101.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2015-04-14
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2017-04-14

This document supersedes EN 60749-26:2006.

EN 60749-26:2014 includes the following significant technical changes with respect to EN 60749-26:2006:

a) descriptions of oscilloscope and current transducers have been refined and updated;

b) the HBM circuit schematic and description have been improved;

c) the description of stress test equipment qualification and verification has been completely re-written;

d) qualification and verification of test fixture boards has been revised;

e) a new section on the determination of ringing in the current waveform has been added;

f) some alternate pin combinations have been included;

g) allowance for non-supply pins to stress to a limited number of supply pin groups (associated non-supply pins) and allowance for non-supply to non-supply (i.e., I/O to I/O) stress to be limited to a finite number of 2 pin pairs (coupled non-supply pin pairs);

h) explicit allowance for HBM stress using 2 pin HBM testers for die only shorted supply groups.

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CONTENTS

FOREWORD ... 4
1 Scope ... 6
2 Normative references ... 6
3 Terms and definitions ... 6
4 Apparatus and required equipment ... 9
4.1 Waveform verification equipment ... 9
4.2 Oscilloscope ... 10
4.3 Additional requirements for digital oscilloscopes ... 10
4.4 Current transducer (inductive current probe) ... 10
4.5 Evaluation loads ... 10
4.6 Human body model simulator ... 10
4.7 HBM test equipment parasitic properties ... 11
5 Stress test equipment qualification and routine verification ... 11
5.1 Overview of required HBM tester evaluations ... 11
5.2 Measurement procedures ... 11
5.2.1 Reference pin pair determination ... 11
5.2.2 Waveform capture with current probe ... 12
5.2.3 Determination of waveform parameters ... 12
5.2.4 High voltage discharge path test ... 15
5.3 HBM tester qualification ... 15
5.3.1 HBM ESD tester qualification requirements ... 15
5.3.2 HBM tester qualification procedure ... 15
5.4 Test fixture board qualification for socketed testers ... 16
5.5 Routine waveform check requirements ... 17
5.5.1 Standard routine waveform check description ... 17
5.5.2 Waveform check frequency ... 17
5.5.3 Alternate routine waveform capture procedure ... 18
5.6 High voltage discharge path check ... 18
5.6.1 Relay testers ... 18
5.6.2 Non-relay testers ... 18
5.7 Tester waveform records ... 18
5.7.1 Tester and test fixture board qualification records ... 18
5.7.2 Periodic waveform check records ... 18
5.8 Safety ... 19
5.8.1 Initial set-up ... 19
5.8.2 Training ... 19
5.8.3 Personnel safety ... 19
6 Classification procedure ... 19
6.1 Devices for classification ... 19
6.2 Parametric and functional testing ... 19
6.3 Device stressing ... 19
6.4 Pin categorization ... 20
6.4.1 General ... 20
6.4.2 No connect pins ... 20
6.4.3 Supply pins ... 20
6.4.4 Non–supply pins ... 21

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6.5 Pin groupings 21
6.5.1 Supply pin groups 21
6.5.2 Shorted non-supply pin groups 22
6.6 Pin stress combinations 22
6.6.1 Pin stress combination categorisation 22
6.6.2 Non-supply and supply to supply combinations (1, 2, … N) 24
6.6.3 Non-supply to non-supply combinations 25
6.7 Testing after stressing 26
7 Failure criteria 26
8 Component classification 26
Annex A (informative) HBM test method flow chart 27
Annex B (informative) HBM test equipment parasitic properties 30
Annex C (informative) Example of testing a product using Table 2, Table 3, or Table 2 with a two-pin HBM tester 34
Annex D (informative) Examples of coupled non-supply pin pairs 40

Figure 1 – Simplified HBM simulator circuit with loads 11
Figure 2 – Current waveform through shorting wires 13
Figure 3 – Current waveform through a 500 Ω resistor 14
Figure 4 – Peak current short circuit ringing waveform 15
Figure B.1 – Diagram of trailing pulse measurement setup 30
Figure B.2 – Positive stress at 4 000 V 31
Figure B.3 – Negative stress at 4 000 V 31
Figure B.4 – Illustration of measuring voltage before HBM pulse with a Zener diode or a device 32
Figure B.5 – Example of voltage rise before the HBM current pulse across a 9,4 V Zener diode 32
Figure C.1 – Example to demonstrate the idea of the partitioned test 35

Table 1 – Waveform specification 17
Table 2 – Preferred pin combinations sets 23
Table 3 – Alternative pin combinations sets 24
Table 4 – HBM ESD component classification levels 26
Table C.1 – Product testing in accordance with Table 2 36
Table C.2 – Product testing in accordance with Table 3 37
Table C.3 – Alternative product testing in accordance with Table 2 38

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

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1 Scope

This standard establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

ESD testing of semiconductor devices is selected from this test method, the machine model (MM) test method (see IEC 60749-27) or other ESD test methods in the IEC 60749 series. The HBM and MM test methods produce similar but not identical results; unless otherwise specified, this test method is the one selected.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-27, *Semiconductor devices – Mechanical and climatic test methods – Part 27: Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
associated non-supply pin
non-supply pin (typically an I/O pin) associated with a supply pin group

Note 1 to entry: A non-supply pin is considered to be associated with a supply pin group if either:

a) The current from the supply pin group (i.e., VDDIO) is required for the function of the electrical circuit(s) (I/O driver) that connect (high/low impedance) to that non-supply pin.

b) A parasitic path exists between non-supply and supply pin group (e.g., open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

3.2
component
item such as a resistor, diode, transistor, integrated circuit or hybrid circuit