



IEC 62680-2-1

Edition 1.0 2015-09

INTERNATIONAL STANDARD



Universal serial bus interfaces for data and power –
Part 2-1: Universal Serial Bus Specification, Revision 2.0





THIS PUBLICATION IS COPYRIGHT PROTECTED
Copyright © 2015 IEC, Geneva, Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester. If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00
info@iec.ch
www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

IEC Catalogue - webstore.iec.ch/catalogue

The stand-alone application for consulting the entire bibliographical information on IEC International Standards, Technical Specifications, Technical Reports and other documents. Available for PC, Mac OS, Android Tablets and iPad.

IEC publications search - www.iec.ch/searchpub

The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee,...). It also gives information on projects, replaced and withdrawn publications.

IEC Just Published - webstore.iec.ch/justpublished

Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and also once a month by email.

Electropedia - www.electropedia.org

The world's leading online dictionary of electronic and electrical terms containing more than 30 000 terms and definitions in English and French, with equivalent terms in 15 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

IEC Glossary - std.iec.ch/glossary

More than 60 000 electrotechnical terminology entries in English and French extracted from the Terms and Definitions clause of IEC publications issued since 2002. Some entries have been collected from earlier publications of IEC TC 37, 77, 86 and CISPR.

IEC Customer Service Centre - webstore.iec.ch/csc

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: csc@iec.ch.



IEC 62680-2-1

Edition 1.0 2015-09

INTERNATIONAL STANDARD



Universal serial bus interfaces for data and power –
Part 2-1: Universal Serial Bus Specification, Revision 2.0

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 29.220; 33.120; 35.200

ISBN 978-2-8322-2845-6

Warning! Make sure that you obtained this publication from an authorized distributor.

INTERNATIONAL ELECTROTECHNICAL COMMISSION

UNIVERSAL SERIAL BUS INTERFACES FOR DATA AND POWER –**Part 2-1: Universal Serial Bus Specification, Revision 2.0****FOREWORD**

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62680-2-1 has been prepared by technical area 14: Interfaces and methods of measurement for personal computing equipment, of IEC technical committee 100: Audio, video and multimedia systems and equipment.

The text of this standard is based on documents prepared by the USB Implementers Forum (USB-IF). The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

The text of this standard is based on the following documents:

CDV	Report on voting
100/2331/CDV	100/2434/RVC

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

A list of all the parts in the IEC 62680 series, published under the general title *Universal serial bus interfaces for data and power* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

The IEC 62680 series is based on a series of specifications that were originally developed by the USB Implementers Forum (USB-IF). These specifications were submitted to the IEC under the auspices of a special agreement between the IEC and the USB IF.

The USB Implementers Forum, Inc.(USB-IF) is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. The Forum facilitates the development of high-quality compatible USB peripherals (devices), and promotes the benefits of USB and the quality of products that have passed compliance testing.

ANY USB SPECIFICATIONS ARE PROVIDED TO YOU "AS IS, "WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE USB IMPLEMENTERS FORUM AND THE AUTHORS OF ANY USB SPECIFICATIONS DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OR IMPLEMENTATION OR INFORMATION IN THIS SPECIFICATION.

THE PROVISION OF ANY USB SPECIFICATIONS TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.

Entering into USB Adopters Agreements may, however, allow a signing company to participate in a reciprocal, royalty-free licensing arrangement for compliant products. For more information, please see:

<http://www.usb.org/developers/docs/>
http://www.usb.org/developers/devclass_docs#approved

IEC DOES NOT TAKE ANY POSITION AS TO WHETHER IT IS ADVISABLE FOR YOU TO ENTER INTO ANY USB ADOPTERS AGREEMENTS OR TO PARTICIPATE IN THE USB IMPLEMENTERS FORUM."

This series covers the Universal Series Bus interfaces for data and power and consists of the following parts:

IEC 62680-1-1, *Universal Serial Bus interfaces for data and power – Part 1-1: Common components – USB Battery Charging Specification, Revision 1.2*

IEC 62680-2-1, *Universal Serial Bus interfaces for data and power – Part 2-1: Universal Serial Bus Specification, Revision 2.0*

IEC 62680-2-2, *Universal Serial Bus interfaces for data and power – Part 2-2: USB Micro-USB Cables and Connectors Specification, Revision 1.01*

IEC 62680-2-3, *Universal Serial Bus interfaces for data and power – Part 2-3: Universal Serial Bus Cables and Connectors Class Document, Revision 2.0*

This part of the IEC 62680 series consists of several distinct parts:

- the main body of the text, which consists of the original specification and all ECN and Errata developed by the USB-IF.

CONTENTS

FOREWORD.....	2
INTRODUCTION.....	4
1 Chapter 1 Introduction	29
1.1 Motivation	29
1.2 Objective of the Specification.....	29
1.3 Scope of the Document.....	30
1.4 USB Product Compliance.....	30
1.5 Document Organization	30
2 Chapter 2 Terms and Abbreviations.....	31
3 Chapter 3 Background.....	37
3.1 Goals for the Universal Serial Bus	37
3.2 Taxonomy of Application Space	37
3.3 Feature List	38
4 Chapter 4 Architectural Overview	40
4.1 USB System Description.....	40
4.1.1 Bus Topology	40
4.2 Physical Interface	41
4.2.1 Electrical	42
4.2.2 Mechanical	42
4.3 Power	42
4.3.1 Power Distribution	43
4.3.2 Power Management.....	43
4.4 Bus Protocol	43
4.5 Robustness.....	43
4.5.1 Error Detection	44
4.5.2 Error Handling	44
4.6 System Configuration.....	44
4.6.1 Attachment of USB Devices.....	44
4.6.2 Removal of USB Devices	44
4.6.3 Bus Enumeration	45
4.7 Data Flow Types	45
4.7.1 Control Transfers	45
4.7.2 Bulk Transfers	45
4.7.3 Interrupt Transfers	45
4.7.4 Isochronous Transfers	46
4.7.5 Allocating USB Bandwidth	46
4.8 USB Devices.....	46
4.8.1 Device Characterizations	46
4.8.2 Device Descriptions	47
4.9 USB Host: Hardware and Software	49
4.10 Architectural Extensions	49
5 Chapter 5 USB Data Flow Model	50
5.1 Implementer Viewpoints	50
5.2 Bus Topology	51
5.2.1 USB Host	52
5.2.2 USB Devices	52

5.2.3	Physical Bus Topology	53
5.2.4	Logical Bus Topology	54
5.2.5	Client Software-to-function Relationship	55
5.3	USB Communication Flow.....	55
5.3.1	Device Endpoints.....	57
5.3.2	Pipes	58
5.3.3	Frames and Microframes	60
5.4	Transfer Types.....	60
5.4.1	Table Calculation Examples.....	61
5.5	Control Transfers	62
5.5.1	Control Transfer Data Format.....	62
5.5.2	Control Transfer Direction.....	63
5.5.3	Control Transfer Packet Size Constraints	63
5.5.4	Control Transfer Bus Access Constraints.....	64
5.5.5	Control Transfer Data Sequences	66
5.6	Isochronous Transfers	67
5.6.1	Isochronous Transfer Data Format.....	67
5.6.2	Isochronous Transfer Direction	67
5.6.3	Isochronous Transfer Packet Size Constraints	67
5.6.4	Isochronous Transfer Bus Access Constraints	69
5.6.5	Isochronous Transfer Data Sequences	70
5.7	Interrupt Transfers	70
5.7.1	Interrupt Transfer Data Format.....	70
5.7.2	Interrupt Transfer Direction.....	70
5.7.3	Interrupt Transfer Packet Size Constraints.....	70
5.7.4	Interrupt Transfer Bus Access Constraints	71
5.7.5	Interrupt Transfer Data Sequences	74
5.8	Bulk Transfers	74
5.8.1	Bulk Transfer Data Format.....	74
5.8.2	Bulk Transfer Direction	74
5.8.3	Bulk Transfer Packet Size Constraints	74
5.8.4	Bulk Transfer Bus Access Constraints	75
5.8.5	Bulk Transfer Data Sequences	76
5.9	High-Speed, High Bandwidth Endpoints	77
5.9.1	High Bandwidth Interrupt Endpoints	77
5.9.2	High Bandwidth Isochronous Endpoints	78
5.10	Split Transactions	79
5.11	Bus Access for Transfers	79
5.11.1	Transfer Management.....	80
5.11.2	Transaction Tracking	82
5.11.3	Calculating Bus Transaction Times	84
5.11.4	Calculating Buffer Sizes in Functions and Software	86
5.11.5	Bus Bandwidth Reclamation	86
5.12	Special Considerations for Isochronous Transfers.....	86
5.12.1	Example Non-USB Isochronous Application	88
5.12.2	USB Clock Model.....	89
5.12.3	Clock Synchronization	91
5.12.4	Isochronous Devices	91
5.12.5	Data Prebuffering	99

5.12.6	SOF Tracking	100
5.12.7	Error Handling	100
5.12.8	Buffering for Rate Matching	101
6	Chapter 6 Mechanical	103
6.1	Architectural Overview	103
6.2	Keyed Connector Protocol	103
6.3	Cable	104
6.4	Cable Assembly	104
6.4.1	Standard Detachable Cable Assemblies	104
6.4.2	High-/full-speed Captive Cable Assemblies	106
6.4.3	Low-speed Captive Cable Assemblies	108
6.4.4	Prohibited Cable Assemblies	110
6.5	Connector Mechanical Configuration and Material Requirements	110
6.5.1	USB Icon Location	111
6.5.2	USB Connector Termination Data	111
6.5.3	Series "A" and Series "B" Receptacles	112
6.5.4	Series "A" and Series "B" Plugs	115
6.6	Cable Mechanical Configuration and Material Requirements	118
6.6.1	Description	119
6.6.2	Construction	119
6.6.3	Electrical Characteristics	122
6.6.4	Cable Environmental Characteristics	122
6.6.5	Listing	122
6.7	Electrical, Mechanical, and Environmental Compliance Standards	123
6.7.1	Applicable Documents	128
6.8	USB Grounding	128
6.9	PCB Reference Drawings	128
7	Chapter 7 Electrical	132
7.1	Signaling	132
7.1.1	USB Driver Characteristics	135
7.1.2	Data Signal Rise and Fall, Eye Patterns	142
7.1.3	Cable Skew	151
7.1.4	Receiver Characteristics	151
7.1.5	Device Speed Identification	153
7.1.6	Input Characteristics	154
7.1.7	Signaling Levels	157
7.1.8	Data Encoding/Decoding	170
7.1.9	Bit Stuffing	170
7.1.10	Sync Pattern	172
7.1.11	Data Signaling Rate	173
7.1.12	Frame Interval	173
7.1.13	Data Source Signaling	174
7.1.14	Hub Signaling Timings	175
7.1.15	Receiver Data Jitter	177
7.1.16	Cable Delay	179
7.1.17	Cable Attenuation	180
7.1.18	Bus Turn-around Time and Inter-packet Delay	181
7.1.19	Maximum End-to-end Signal Delay	182
7.1.20	Test Mode Support	183

7.2	Power Distribution	184
7.2.1	Classes of Devices	184
7.2.2	Voltage Drop Budget	189
7.2.3	Power Control During Suspend/Resume	189
7.2.4	Dynamic Attach and Detach.....	190
7.3	Physical Layer	191
7.3.1	Regulatory Requirements	191
7.3.2	Bus Timing/Electrical Characteristics	192
7.3.3	Timing Waveforms	202
8	Chapter 8 Protocol Layer.....	205
8.1	Byte/Bit Ordering	205
8.2	SYNC Field.....	205
8.3	Packet Field Formats	205
8.3.1	Packet Identifier Field	205
8.3.2	Address Fields.....	206
8.3.3	Frame Number Field.....	207
8.3.4	Data Field.....	207
8.3.5	Cyclic Redundancy Checks.....	208
8.4	Packet Formats.....	209
8.4.1	Token Packets	209
8.4.2	Split Transaction Special Token Packets	209
8.4.3	Start-of-Frame Packets	214
8.4.4	Data Packets	215
8.4.5	Handshake Packets	216
8.4.6	Handshake Responses	217
8.5	Transaction Packet Sequences	218
8.5.1	NAK Limiting via Ping Flow Control.....	227
8.5.2	Bulk Transactions	231
8.5.3	Control Transfers.....	236
8.5.4	Interrupt Transactions	239
8.5.5	Isochronous Transactions	239
8.6	Data Toggle Synchronization and Retry	243
8.6.1	Initialization via SETUP Token.....	244
8.6.2	Successful Data Transactions.....	244
8.6.3	Data Corrupted or Not Accepted	245
8.6.4	Corrupted ACK Handshake.....	245
8.6.5	Low-speed Transactions	246
8.7	Error Detection and Recovery	247
8.7.1	Packet Error Categories	247
8.7.2	Bus Turn-around Timing	247
8.7.3	False EOPs	248
8.7.4	Babble and Loss of Activity Recovery	249
9	Chapter 9 USB Device Framework.....	250
9.1	USB Device States	250
9.1.1	Visible Device States.....	250
9.1.2	Bus Enumeration	254
9.2	Generic USB Device Operations	254
9.2.1	Dynamic Attachment and Removal	255
9.2.2	Address Assignment.....	255

9.2.3	Configuration	255
9.2.4	Data Transfer	256
9.2.5	Power Management.....	256
9.2.6	Request Processing.....	256
9.2.7	Request Error	258
9.3	USB Device Requests.....	259
9.3.1	bmRequestType	259
9.3.2	bRequest	259
9.3.3	wValue	259
9.3.4	wIndex.....	260
9.3.5	wLength.....	260
9.4	Standard Device Requests.....	260
9.4.1	Clear Feature	262
9.4.2	Get Configuration	263
9.4.3	Get Descriptor.....	263
9.4.4	Get Interface	264
9.4.5	Get Status	264
9.4.6	Set Address.....	266
9.4.7	Set Configuration.....	266
9.4.8	Set Descriptor	267
9.4.9	Set Feature	268
9.4.10	Set Interface.....	269
9.4.11	Synch Frame	269
9.5	Descriptors	270
9.6	Standard USB Descriptor Definitions.....	270
9.6.1	Device	270
9.6.2	Device_Qualifier	272
9.6.3	Configuration.....	273
9.6.4	Other_Speed_Configuration	275
9.6.5	Interface	275
9.6.6	Endpoint	276
9.6.7	String	279
9.7	Device Class Definitions	280
9.7.1	Descriptors	280
9.7.2	Interface(s) and Endpoint Usage	280
9.7.3	Requests	281
10	Chapter 10 USB Host: Hardware and Software.....	282
10.1	Overview of the USB Host.....	282
10.1.1	Overview	282
10.1.2	Control Mechanisms	285
10.1.3	Data Flow	285
10.1.4	Collecting Status and Activity Statistics	286
10.1.5	Electrical Interface Considerations	286
10.2	Host Controller Requirements	286
10.2.1	State Handling.....	287
10.2.2	Serializer/Deserializer	287
10.2.3	Frame and Microframe Generation	287
10.2.4	Data Processing	288
10.2.5	Protocol Engine	288

10.2.6	Transmission Error Handling.....	288
10.2.7	Remote Wakeup	289
10.2.8	Root Hub	289
10.2.9	Host System Interface	289
10.3	Overview of Software Mechanisms.....	289
10.3.1	Device Configuration	290
10.3.2	Resource Management.....	292
10.3.3	Data Transfers.....	292
10.3.4	Common Data Definitions	293
10.4	Host Controller Driver	293
10.5	Universal Serial Bus Driver	294
10.5.1	USBD Overview	294
10.5.2	USBD Command Mechanism Requirements	296
10.5.3	USBD Pipe Mechanisms	298
10.5.4	Managing the USB via the USBD Mechanisms.....	300
10.5.5	Passing USB Preboot Control to the Operating System	302
10.6	Operating System Environment Guides	302
11	Chapter 11 Hub Specification.....	303
11.1	Overview	303
11.1.1	Hub Architecture.....	303
11.1.2	Hub Connectivity	304
11.2	Hub Frame/Microframe Timer.....	306
11.2.1	High-speed Microframe Timer Range.....	306
11.2.2	Full-speed Frame Timer Range.....	306
11.2.3	Frame/Microframe Timer Synchronization.....	307
11.2.4	Microframe Jitter Related to Frame Jitter.....	309
11.2.5	EOF1 and EOF2 Timing Points	309
11.3	Host Behavior at End-of-Frame	312
11.3.1	Full-/low-speed Latest Host Packet.....	312
11.3.2	Full-/low-speed Packet Nullification	312
11.3.3	Full-/low-speed Transaction Completion Prediction.....	313
11.4	Internal Port.....	313
11.4.1	Inactive.....	314
11.4.2	Suspend Delay	314
11.4.3	Full Suspend (Fsus)	314
11.4.4	Generate Resume (GResume).....	314
11.5	Downstream Facing Ports	315
11.5.1	Downstream Facing Port State Descriptions	317
11.5.2	Disconnect Detect Timer.....	321
11.5.3	Port Indicator.....	322
11.6	Upstream Facing Port	324
11.6.1	Full-speed	324
11.6.2	High-speed	325
11.6.3	Receiver	325
11.6.4	Transmitter	328
11.7	Hub Repeater	330
11.7.1	High-speed Packet Connectivity	330
11.7.2	Hub Repeater State Machine	332
11.7.3	Wait for Start of Packet from Upstream Port (WFSOPFU).....	334

11.7.4	Wait for End of Packet from Upstream Port (WFEOPFU)	334
11.7.5	Wait for Start of Packet (WFSOP).....	334
11.7.6	Wait for End of Packet (WFEOP)	334
11.8	Bus State Evaluation.....	335
11.8.1	Port Error	335
11.8.2	Speed Detection	335
11.8.3	Collision	336
11.8.4	Low-speed Port Behavior.....	336
11.9	Suspend and Resume.....	337
11.10	Hub Reset Behavior	339
11.11	Hub Port Power Control	339
11.11.1	Multiple Gangs	340
11.12	Hub Controller	340
11.12.1	Endpoint Organization	341
11.12.2	Hub Information Architecture and Operation	341
11.12.3	Port Change Information Processing.....	342
11.12.4	Hub and Port Status Change Bitmap.....	343
11.12.5	Over-current Reporting and Recovery.....	344
11.12.6	Enumeration Handling.....	345
11.13	Hub Configuration	345
11.14	Transaction Translator	346
11.14.1	Overview	347
11.14.2	Transaction Translator Scheduling.....	349
11.15	Split Transaction Notation Information	351
11.16	Common Split Transaction State Machines	354
11.16.1	Host Controller State Machine	355
11.16.2	Transaction Translator State Machine.....	359
11.17	Bulk/Control Transaction Translation Overview	364
11.17.1	Bulk/Control Split Transaction Sequences	365
11.17.2	Bulk/Control Split Transaction State Machines.....	371
11.17.3	Bulk/Control Sequencing	376
11.17.4	Bulk/Control Buffering Requirements	377
11.17.5	Other Bulk/Control Details	377
11.18	Periodic Split Transaction Pipelining and Buffer Management	377
11.18.1	Best Case Full-Speed Budget.....	378
11.18.2	TT Microframe Pipeline.....	378
11.18.3	Generation of Full-speed Frames.....	379
11.18.4	Host Split Transaction Scheduling Requirements	379
11.18.5	TT Response Generation	382
11.18.6	TT Periodic Transaction Handling Requirements	383
11.18.7	TT Transaction Tracking	385
11.18.8	TT Complete-split Transaction State Searching	386
11.19	Approximate TT Buffer Space Required	387
11.20	Interrupt Transaction Translation Overview	387
11.20.1	Interrupt Split Transaction Sequences	388
11.20.2	Interrupt Split Transaction State Machines.....	391
11.20.3	Interrupt OUT Sequencing	397
11.20.4	Interrupt IN Sequencing	398
11.21	Isochronous Transaction Translation Overview	399

11.21.1	Isochronous Split Transaction Sequences	400
11.21.2	Isochronous Split Transaction State Machines	403
11.21.3	Isochronous OUT Sequencing	406
11.21.4	Isochronous IN Sequencing	407
11.22	TT Error Handling	408
11.22.1	Loss of TT Synchronization With HS SOFs	408
11.22.2	TT Frame and Microframe Timer Synchronization Requirements	409
11.23	Descriptors	410
11.23.1	Standard Descriptors for Hub Class	411
11.23.2	Class-specific Descriptors	419
11.24	Requests	420
11.24.1	Standard Requests	420
11.24.2	Class-specific Requests	421
Appendix A	Transaction Examples	437
A.1	Bulk/Control OUT and SETUP Transaction Examples	437
A.2	Bulk/Control IN Transaction Examples	461
A.3	Interrupt OUT Transaction Examples	485
A.4	Interrupt IN Transaction Examples	504
A.5	Isochronous OUT Split-transaction Examples	526
A.6	Isochronous IN Split-transaction Examples	535
Appendix B	Example Declarations for State Machines	549
B.1	Global Declarations	550
B.2	Host Controller Declarations	553
B.3	Transaction Translator Declarations	555
Appendix C	Reset Protocol State Diagrams	559
C.1	Downstream Facing Port State Diagram	559
C.2	Upstream Facing Port State Diagram	561
C.2.1	Reset From Suspended State	561
C.2.2	Reset From Full-speed Non-suspended State	564
C.2.3	Reset From High-speed Non-suspended State	564
C.2.4	Reset Handshake	564
Figure 3-1	– Application Space Taxonomy	37
Figure 4-1	– Bus Topology	41
Figure 4-2	– USB Cable	42
Figure 4-3	– A Typical Hub	47
Figure 4-4	– Hubs in a Desktop Computer Environment	48
Figure 5-1	– Simple USB Host/Device View	50
Figure 5-2	– USB Implementation Areas	51
Figure 5-3	– Host Composition	52
Figure 5-4	– Physical Device Composition	53
Figure 5-5	– USB Physical Bus Topology	53
Figure 5-6	– Multiple Full-speed Buses in a High-speed System	54
Figure 5-7	– USB Logical Bus Topology	55
Figure 5-8	– Client Software-to-function Relationships	55
Figure 5-9	– USB Host/Device Detailed View	56

Figure 5-10 – USB Communication Flow	57
Figure 5-11 – Data Phase PID Sequence for Isochronous IN High Bandwidth Endpoints.....	78
Figure 5-12 – Data Phase PID Sequence for Isochronous OUT High Bandwidth Endpoints	79
Figure 5-13 – USB Information Conversion From Client Software to Bus.....	80
Figure 5-14 – Transfers for Communication Flows	83
Figure 5-15 – Arrangement of IRPs to Transactions/(Micro)frames	84
Figure 5-16 – Non-USB Isochronous Example	88
Figure 5-17 – USB Full-speed Isochronous Application	90
Figure 5-18 – Example Source/Sink Connectivity	96
Figure 5-19 – Data Prebuffering	100
Figure 5-20 – Packet and Buffer Size Formulas for Rate-matched Isochronous Transfers	102
Figure 6-1 – Keyed Connector Protocol	103
Figure 6-2 – USB Standard Detachable Cable Assembly	105
Figure 6-3 – USB High-/full-speed Hardwired Cable Assembly.....	107
Figure 6-4 – USB Low-speed Hardwired Cable Assembly	109
Figure 6-5 – USB Icon	111
Figure 6-6 – Typical USB Plug Orientation.....	111
Figure 6-7 – USB Series "A" Receptacle Interface and Mating Drawing	113
Figure 6-8 – USB Series "B" Receptacle Interface and Mating Drawing	114
Figure 6-9 – USB Series "A" Plug Interface Drawing	116
Figure 6-10 – USB Series "B" Plug Interface Drawing	117
Figure 6-11 – Typical High-/full-speed Cable Construction	119
Figure 6-12 – Single Pin-type Series "A" Receptacle.....	129
Figure 6-13 – Dual Pin-type Series "A" Receptacle	130
Figure 6-14 – Single Pin-type Series "B" Receptacle.....	131
Figure 7-1 – Example High-speed Capable Transceiver Circuit	132
Figure 7-2 – Maximum Input Waveforms for USB Signaling	135
Figure 7-3 – Example Full-speed CMOS Driver Circuit (non High-speed capable)	136
Figure 7-4 – Full-speed Buffer V/I Characteristics	138
Figure 7-5 – Full-speed Buffer V/I Characteristics for High-speed Capable Transceiver	139
Figure 7-6 – Full-speed Signal Waveforms.....	140
Figure 7-7 – Low-speed Driver Signal Waveforms.....	140
Figure 7-8 – Data Signal Rise and Fall Time	142
Figure 7-9 – Full-speed Load	143
Figure 7-10 – Low-speed Port Loads	143
Figure 7-11 – Measurement Planes	143
Figure 7-12 – Transmitter/Receiver Test Fixture	144
Figure 7-13 – Template 1.....	145
Figure 7-14 – Template 2.....	146
Figure 7-15 – Template 3.....	147
Figure 7-16 – Template 4.....	148
Figure 7-17 – Template 5.....	149

Figure 7-18 – Template 6.....	150
Figure 7-19 – Differential Input Sensitivity Range for Low-/full-speed.....	152
Figure 7-20 – Full-speed Device Cable and Resistor Connections	153
Figure 7-21 – Low-speed Device Cable and Resistor Connections.....	154
Figure 7-22 – Placement of Optional Edge Rate Control Capacitors for Low-/full-speed.....	155
Figure 7-23 – Diagram for High-speed Loading Equivalent Circuit.....	155
Figure 7-24 – Upstream Facing Full-speed Port Transceiver	159
Figure 7-25 – Downstream Facing Low-/full-speed Port Transceiver	159
Figure 7-26 – Low-/full-speed Disconnect Detection.....	162
Figure 7-27 – Full-/high-speed Device Connect Detection	162
Figure 7-28 – Low-speed Device Connect Detection	162
Figure 7-29 – Power-on and Connection Events Timing	163
Figure 7-30 – Low-/full-speed Packet Voltage Levels	165
Figure 7-31 – NRZI Data Encoding	170
Figure 7-32 – Bit Stuffing	171
Figure 7-33 – Illustration of Extra Bit Preceding EOP (Full-/low-speed).....	171
Figure 7-34 – Flow Diagram for Bit Stuffing.....	172
Figure 7-35 – Sync Pattern (Low-/full-speed)	172
Figure 7-36 – Data Jitter Taxonomy	174
Figure 7-37 – SE0 for EOP Width Timing	175
Figure 7-38 – Hub Propagation Delay of Full-speed Differential Signals	176
Figure 7-39 – Full-speed Cable Delay	180
Figure 7-40 – Low-speed Cable Delay	180
Figure 7-41 – Worst-case End-to-end Signal Delay Model for Low-/full-speed.....	183
Figure 7-42 – Compound Bus-powered Hub.....	186
Figure 7-43 – Compound Self-powered Hub.....	187
Figure 7-44 – Low-power Bus-powered Function.....	188
Figure 7-45 – High-power Bus-powered Function.....	188
Figure 7-46 – Self-powered Function	189
Figure 7-47 – Worst-case Voltage Drop Topology (Steady State)	189
Figure 7-48 – Typical Suspend Current Averaging Profile	190
Figure 7-49 – Differential Data Jitter for Low-/full-speed	202
Figure 7-50 – Differential-to-EOP Transition Skew and EOP Width for Low-/full-speed	202
Figure 7-51 – Receiver Jitter Tolerance for Low-/full-speed	202
Figure 7-52 – Hub Differential Delay, Differential Jitter, and SOP Distortion for Low-/full-speed.....	203
Figure 7-53 – Hub EOP Delay and EOP Skew for Low-/full-speed.....	204
Figure 8-1 – PID Format	205
Figure 8-2 – ADDR Field	207
Figure 8-3 – Endpoint Field.....	207
Figure 8-4 – Data Field Format	208
Figure 8-5 – Token Format	209
Figure 8-6 – Packets in a Start-split Transaction	210

Figure 8-7 – Packets in a Complete-split Transaction	210
Figure 8-8 – Relationship of Interrupt IN Transaction to High-speed Split Transaction	211
Figure 8-9 – Relationship of Interrupt OUT Transaction to High-speed Split OUT Transaction.....	211
Figure 8-10 – Start-split (SSPLIT) Token	212
Figure 8-11 – Port Field	212
Figure 8-12 – Complete-split (CSPLIT) Transaction Token.....	214
Figure 8-13 – SOF Packet	214
Figure 8-14 – Relationship between Frames and Microframes	215
Figure 8-15 – Data Packet Format	216
Figure 8-16 – Handshake Packet	216
Figure 8-17 – Legend for State Machines.....	219
Figure 8-18 – State Machine Context Overview.....	220
Figure 8-19 – Host Controller Top Level Transaction State Machine Hierarchy Overview	220
Figure 8-20 – Host Controller Non-split Transaction State Machine Hierarchy Overview	221
Figure 8-21 – Device Transaction State Machine Hierarchy Overview.....	221
Figure 8-22 – Device Top Level State Machine	222
Figure 8-23 – Device_process_Trans State Machine.....	223
Figure 8-24 – Dev_do_OUT State Machine.....	224
Figure 8-25 – Dev_do_IN State Machine.....	225
Figure 8-26 – HC_Do_nonsplit State Machine.....	226
Figure 8-27 – Host High-speed Bulk OUT/Control Ping State Machine	228
Figure 8-28 – Dev_HS_ping State Machine.....	229
Figure 8-29 – Device High-speed Bulk OUT /Control State Machine	230
Figure 8-30 – Bulk Transaction Format	231
Figure 8-31 – Bulk/Control/Interrupt OUT Transaction Host State Machine	232
Figure 8-32 – Bulk/Control/Interrupt OUT Transaction Device State Machine	233
Figure 8-33 – Bulk/Control/Interrupt IN Transaction Host State Machine	234
Figure 8-34 – Bulk/Control/Interrupt IN Transaction Device State Machine.....	235
Figure 8-35 – Bulk Reads and Writes	235
Figure 8-36 – Control SETUP Transaction	236
Figure 8-37 – Control Read and Write Sequences.....	237
Figure 8-38 – Interrupt Transaction Format.....	239
Figure 8-39 – Isochronous Transaction Format	240
Figure 8-40 – Isochronous OUT Transaction Host State Machine.....	241
Figure 8-41 – Isochronous OUT Transaction Device State Machine	241
Figure 8-42 – Isochronous IN Transaction Host State Machine	242
Figure 8-43 – Isochronous IN Transaction Device State Machine	243
Figure 8-44 – SETUP Initialization	244
Figure 8-45 – Consecutive Transactions	244
Figure 8-46 – NAKed Transaction with Retry.....	245
Figure 8-47 – Corrupted ACK Handshake with Retry.....	245
Figure 8-48 – Low-speed Transaction	246

Figure 8-49 – Bus Turn-around Timer Usage	248
Figure 9-1 – Device State Diagram	251
Figure 9-2 – wIndex Format when Specifying an Endpoint	260
Figure 9-3 – wIndex Format when Specifying an Interface	260
Figure 9-4 – Information Returned by a GetStatus() Request to a Device	265
Figure 9-5 – Information Returned by a GetStatus() Request to an Interface	265
Figure 9-6 – Information Returned by a GetStatus() Request to an Endpoint	265
Figure 9-7 – Example of Feedback Endpoint Numbers	279
Figure 9-8 – Example of Feedback Endpoint Relationships	279
Figure 10-1 – Interlayer Communications Model	282
Figure 10-2 – Host Communications	283
Figure 10-3 – Frame and Microframe Creation	287
Figure 10-4 – Configuration Interactions	290
Figure 10-5 – Universal Serial Bus Driver Structure	295
Figure 11-1 – Hub Architecture	304
Figure 11-2 – Hub Signaling Connectivity	305
Figure 11-3 – Resume Connectivity	305
Figure 11-4 – Example High-speed EOF Offsets Due to Propagation Delay Without EOF Advancement	308
Figure 11-5 – Example High-speed EOF Offsets Due to Propagation Delay With EOF Advancement	308
Figure 11-6 – High-speed EOF2 Timing Point	310
Figure 11-7 – High-speed EOF1 Timing Point	310
Figure 11-8 – Full-speed EOF Timing Points	310
Figure 11-9 – Internal Port State Machine	314
Figure 11-10 – Downstream Facing Hub Port State Machine	316
Figure 11-11 – Port Indicator State Diagram	323
Figure 11-12 – Upstream Facing Port Receiver State Machine	325
Figure 11-13 – Upstream Facing Port Transmitter State Machine	328
Figure 11-14 – Example Hub Repeater Organization	330
Figure 11-15 – High-speed Port Selector State Machine	331
Figure 11-16 – Hub Repeater State Machine	333
Figure 11-17 – Example Remote-wakeup Resume Signaling With Full-/low-speed Device	338
Figure 11-18 – Example Remote-wakeup Resume Signaling With High-speed Device	338
Figure 11-19 – Example Hub Controller Organization	341
Figure 11-20 – Relationship of Status, Status Change, and Control Information to Device States	342
Figure 11-21 – Port Status Handling Method	343
Figure 11-22 – Hub and Port Status Change Bitmap	344
Figure 11-23 – Example Hub and Port Change Bit Sampling	344
Figure 11-24 – Transaction Translator Overview	347
Figure 11-25 – Periodic and Non-periodic Buffer Sections of TT	348
Figure 11-26 – TT Microframe Pipeline for Periodic Split Transactions	349

Figure 11-27 – TT Nonperiodic Buffering	350
Figure 11-28 – Example Full-/low-speed Handler Scheduling for Start-splits	351
Figure 11-29 – Flow Sequence Legend	351
Figure 11-30 – Legend for State Machines.....	352
Figure 11-31 – State Machine Context Overview.....	354
Figure 11-32 – Host Controller Split Transaction State Machine Hierarchy Overview	354
Figure 11-33 – Transaction Translator State Machine Hierarchy Overview.....	355
Figure 11-34 – Host Controller	355
Figure 11-35 – HC_Process_Command	356
Figure 11-36 – HC_Do_Start.....	357
Figure 11-37 – HC_Do_Complete	358
Figure 11-38 – Transaction Translator	359
Figure 11-39 – TT_Process_Packet	360
Figure 11-40 – TT_Do_Start	361
Figure 11-41 – TT_Do_Complete	362
Figure 11-42 – TT_BulkSS.....	362
Figure 11-43 – TT_BulkCS.....	363
Figure 11-44 – TT_IntSS.....	363
Figure 11-45 – TT_IntCS	364
Figure 11-46 – TT_IsochSS	364
Figure 11-47 – Sample Algorithm for Compare_buffs	366
Figure 11-48 – Bulk/Control OUT Start-split Transaction Sequence	367
Figure 11-49 – Bulk/Control OUT Complete-split Transaction Sequence	368
Figure 11-50 – Bulk/Control IN Start-split Transaction Sequence	369
Figure 11-51 – Bulk/Control IN Complete-split Transaction Sequence.....	370
Figure 11-52 – Bulk/Control OUT Start-split Transaction Host State Machine.....	371
Figure 11-53 – Bulk/Control OUT Complete-split Transaction Host State Machine	372
Figure 11-54 – Bulk/Control OUT Start-split Transaction TT State Machine	373
Figure 11-55 – Bulk/Control OUT Complete-split Transaction TT State Machine	373
Figure 11-56 – Bulk/Control IN Start-split Transaction Host State Machine	374
Figure 11-57 – Bulk/Control IN Complete-split Transaction Host State Machine	375
Figure 11-58 – Bulk/Control IN Start-split Transaction TT State Machine	376
Figure 11-59 – Bulk/Control IN Complete-split Transaction TT State Machine	376
Figure 11-60 – Best Case Budgeted Full-speed Wire Time With No Bit Stuffing.....	378
Figure 11-61 – Scheduling of TT Microframe Pipeline	379
Figure 11-62 – Isochronous OUT Example That Avoids a Start-split-end With Zero Data.....	380
Figure 11-63 – End of Frame TT Pipeline Scheduling Example	381
Figure 11-64 – Isochronous IN Complete-split Schedule Example at L=Y ₆	381
Figure 11-65 – Isochronous IN Complete-split Schedule Example at L=Y ₇	382
Figure 11-66 – Microframe Pipeline	385
Figure 11-67 – Advance_Pipeline Pseudocode	386
Figure 11-68 – Interrupt OUT Start-split Transaction Sequence	388

Figure 11-69 – Interrupt OUT Complete-split Transaction Sequence	389
Figure 11-70 – Interrupt IN Start-split Transaction Sequence	389
Figure 11-71 – Interrupt IN Complete-split Transaction Sequence	390
Figure 11-72 – Interrupt OUT Start-split Transaction Host State Machine	391
Figure 11-73 – Interrupt OUT Complete-split Transaction Host State Machine	392
Figure 11-74 – Interrupt OUT Start-split Transaction TT State Machine	393
Figure 11-75 – Interrupt OUT Complete-split Transaction TT State Machine	393
Figure 11-76 – Interrupt IN Start-split Transaction Host State Machine	394
Figure 11-77 – Interrupt IN Complete-split Transaction Host State Machine	395
Figure 11-78 – HC_Data_or_Error State Machine	396
Figure 11-79 – Interrupt IN Start-split Transaction TT State Machine	396
Figure 11-80 – Interrupt IN Complete-split Transaction TT State Machine	397
Figure 11-81 – Example of CRC16 Handling for Interrupt OUT	398
Figure 11-82 – Example of CRC16 Handling for Interrupt IN	399
Figure 11-83 – Isochronous OUT Start-split Transaction Sequence	401
Figure 11-84 – Isochronous IN Start-split Transaction Sequence	401
Figure 11-85 – Isochronous IN Complete-split Transaction Sequence	402
Figure 11-86 – Isochronous OUT Start-split Transaction Host State Machine	403
Figure 11-87 – Isochronous OUT Start-split Transaction TT State Machine	404
Figure 11-88 – Isochronous IN Start-split Transaction Host State Machine	405
Figure 11-89 – Isochronous IN Complete-split Transaction Host State Machine	405
Figure 11-90 – Isochronous IN Start-split Transaction TT State Machine	406
Figure 11-91 – Isochronous IN Complete-split Transaction TT State Machine	406
Figure 11-92 – Example of CRC16 Isochronous OUT Data Packet Handling	407
Figure 11-93 – Example of CRC16 Isochronous IN Data Packet Handling	408
Figure 11-94 – Example Frame/Microframe Synchronization Events	410
Figure A-1 – Normal No Smash	438
Figure A-2 – Normal HS DATA0/1 Smash	439
Figure A-3 – Normal HS DATA0/1 3 Strikes Smash	440
Figure A-4 – Normal HS ACK(S) Smash (case 1)	441
Figure A-5 – Normal HS ACK(S) Smash (case 2)	442
Figure A-6 – Normal HS ACK(S) 3 Strikes Smash	443
Figure A-7 – Normal HS CSPLIT Smash	444
Figure A-8 – Normal HS CSPLIT 3 Strikes Smash	445
Figure A-9 – Normal HS ACK(C) Smash	446
Figure A-10 – Normal S ACK(C) 3 Strikes Smash	447
Figure A-11 – Normal FS/LS DATA0/1 Smash	448
Figure A-12 – Normal FS/LS DATA0/1 3 Strikes Smash	449
Figure A-13 – Normal FS/LS ACK Smash	450
Figure A-14 – Normal FS/LS ACK 3 Strikes Smash	451
Figure A-15 – No buffer Available No Smash (HS NAK(S))	452
Figure A-16 – No Buffer Available HS NAK(S) Smash	453
Figure A-17 – No Buffer Available HS NAK(S) 3 Strikes Smash	454

Figure A-18 – CS Earlier No Smash (HS NYET).....	455
Figure A-19 – CS Earlier HS NYET Smash (case 1).....	456
Figure A-20 – CS Earlier HS NYET Smash (case 2).....	457
Figure A-21 – CS Earlier HS NYET 3 Strikes Smash.....	458
Figure A-22 – Device Busy No Smash(FS/LS NAK).....	459
Figure A-23 – Device Stall No Smash(FS/LS STALL).....	460
Figure A-24 – Normal No Smash.....	462
Figure A-25 – Normal HS SSPLIT Smash	463
Figure A-26 – Normal SSPLIT 3 Strikes Smash	464
Figure A-27 – Normal HS ACK(S) Smash (case 1).....	465
Figure A-28 – Normal HS ACK(S) Smash (case 2).....	466
Figure A-29 – Normal HS ACK(S) 3 Strikes Smash	467
Figure A-30 – Normal HS CSPLIT Smash	468
Figure A-31 – Normal HS CSPLIT 3 Strikes Smash.....	469
Figure A-32 – Normal HS DATA0/1 Smash	470
Figure A-33 – Normal HS DATA0/1 3 Strikes Smash.....	471
Figure A-34 – Normal FS/LS IN Smash	472
Figure A-35 – Normal FS/LS IN 3 Strikes Smash	473
Figure A-36 – Normal FS/LS DATA0/1 Smash	474
Figure A-37 – Normal FS/LS DATA0/1 3 Strikes Smash	475
Figure A-38 – Normal FS/LS ACK Smash	476
Figure A-39 – No Buffer Available No Smash(HS NAK(S))	477
Figure A-40 – No Buffer Available HS NAK(S) Smash	478
Figure A-41 – No Buffer Available HS NAK(S) 3 Strikes Smash	479
Figure A-42 – CS Earlier No Smash (HS NYET).....	480
Figure A-43 – CS Earlier HS NYET Smash (case 1).....	481
Figure A-44 – CS Earlier HS NYET Smash (case 2).....	482
Figure A-45 – Device Busy No Smash(FS/LS NAK).....	483
Figure A-46 – Device Stall No Smash(FS/LS STALL).....	484
Figure A-47 – Normal No Smash(FS/LS Handshake Packet is Done by M+1).....	487
Figure A-48 – Normal HS DATA0/1 Smash	488
Figure A-49 – Normal HS CSPLIT Smash	489
Figure A-50 – Normal HS CSPLIT 3 Strikes Smash.....	490
Figure A-51 – Normal HS ACK(C) Smash	491
Figure A-52 – Normal HS ACK(C) 3 Strikes Smash.....	492
Figure A-53 – Normal FS/LS DATA0/1 Smash	493
Figure A-54 – Normal FS/LS ACK Smash	494
Figure A-55 – Searching No Smash	495
Figure A-56 – CS Earlier No Smash(HS NYET and FS/LS Handshake Packet is Done by M+2)	496
Figure A-57 – CS Earlier No Smash(HS NYET and FS/LS Handshake Packet is Done by M+3)	497
Figure A-58 – CS Earlier HS NYET Smash	498
Figure A-59 – CS Earlier HS NYET 3 Strikes Smash.....	499

Figure A-60 – Abort and Free Abort(FS/LS Transaction is Continued at End of M+3)	500
Figure A-61 – Abort and Free Free(FS/LS Transaction is not Started at End of M+3)	501
Figure A-62 – Device Busy No Smash(FS/LS NAK).....	502
Figure A-63 – Device Stall No Smash(FS/LS STALL).....	503
Figure A-64 – Normal No Smash (FS/LS Data Packet is on M+1).....	506
Figure A-65 – Normal HS SSPLIT Smash	507
Figure A-66 – Normal HS CSPLIT Smash	508
Figure A-67 – Normal HS CSPLIT 3 Strikes Smash.....	509
Figure A-68 – Normal HS DATA0/1 Smash	510
Figure A-69 – Normal HS DATA0/1 3 Strikes Smash.....	511
Figure A-70 – Normal FS/LS IN Smash	512
Figure A-71 – Normal FS/LS DATA0/1 Smash	513
Figure A-72 – Normal FS/LS ACK Smash	514
Figure A-73 – Searching No Smash	515
Figure A-74 – CS Earlier No Smash (HS MDATA and FS/LS Data Packet is on M+1 and M+2)	516
Figure A-75 – CS Earlier No Smash (HS NYET and FS/LS Data Packet is on M+2)	517
Figure A-76 – CS Earlier No Smash (HS NYET and MDATA and FS/LS Data Packet is on M+2 and M+3).....	518
Figure A-77 – CS Earlier No Smash(HS NYET and FS/LS Data Packet is on M+3)	519
Figure A-78 – CS Earlier HS NYET Smash	520
Figure A-79 – CS Earlier HS NYET 3 Strikes Smash.....	521
Figure A-80 – Abort and Free Abort (HS NYET and FS/LS Transaction is Continued at End of M+3).....	522
Figure A-81 – Abort and Free Free (HS NYET and FS/LS Transaction is not Started at End of M+3)	523
Figure A-82 – Device Busy No Smash(FS/LS NAK).....	524
Figure A-83 – Device Stall No Smash(FS/LS STALL).....	525
Figure C-1 – Downstream Facing Port Reset Protocol State Diagram	560
Figure C-2 – Upstream Facing Port Reset Detection State Diagram	562
Figure C-3 – Upstream Facing Port Reset Handshake State Diagram	563
Figure 8-27 – Host High-speed Bulk OUT/Control Ping State Machine	643
Figure 8-31 – FS Bulk, FS/LS/ Control, or HS/FS/LS Interrupt/ OUT Transaction Host State Machine.....	644
Figure 8-32 – FS Bulk, /FS/LS Control, /or HS/FS/LS Interrupt OUT Transaction Host State Machine	645
Figure11-11 – Port Indicator State Diagram	661
Figure 6-1 – Keyed Connector Protocol	670
Figure 6-2 – USB Standard Detachable Cable Assembly	672
Figure 6-3 – USB Standard Mini-connector Detachable Cable Assembly.....	673
Figure 6-3 – USB High-/full-speed Hardwired Cable Assembly.....	675
Figure 6-46-5 – USB Low-speed Hardwired Cable Assembly	677
Figure 6-56-6 – USB Icon	679
Figure 6-66-7 – Typical USB Plug Orientation.....	680

Figure 6-8 – Typical USB “Mini-B” Connector Plug Orientation.....	681
Figure 6-76-9 – USB Series "A" Receptacle Interface and Mating Drawing	683
Figure 6-86-10 – USB Series "B" Receptacle Interface and Mating Drawing.....	684
Figure 6-11 – USB Series "Mini-B" Receptacle Interface and Mating Drawing	685
Figure 6-12 – USB Series “Mini-B” Receptacle Interface Drawing (Detail).tiff	686
Figure 6-96-13 – USB Series "A" Plug Interface Drawing	689
Figure 6-106-14 – USB Series “B” Plug Interface Drawing	690
Figure 6-15 – USB Series “Mini-B” Plug Interface Drawing	691
Figure 6-116-16 – Typical High-/full-speed Cable Construction	694
Figure 6-126-17 – Single Pin-type Series "A" Receptacle.....	704
Figure 6-136-18 – Dual Pin-type Series "A" Receptacle	705
Figure 6-146-19 – Single Pin-type Series "B" Receptacle.....	706
Figure 6-20 – Single Pin Type Series “Mini-B” Receptacle	707
Figure 11-11 – Port Indicator State Diagram	720
Figure 11-82 – Example of CRC16 Handling for Interrupt IN	725
Figure 11-93 – Example of CRC16 Isochronous IN Data Packet Handling	725
Figure 6-15 – USB Series “Mini-B” Plug Interface Drawing (1 of 2)	736
Figure 6-15 – USB Series “Mini-B” Plug Interface Drawing (2 of 2)	737
Figure 1-1 – LPM State Transition Diagram	744
Figure 2-1 – Packets in an Extension Token Transaction	746
Figure 2-2 – LPM Extended Token.....	747
Figure 2-3 – LPM Transaction Format	748
Figure 4-1 – Port Control Model for Transitioning a Port to L1	751
Figure 4-2 – LPM Transaction and Transition Timing to L1	752
Figure 4-3 – Device Initiated L1 to L0 Transition (Remote Wake).....	753
Figure 4-4 – Example Remote-wakeup L1 Exit with Full-speed Device Under Connected Hub	754
Figure 4-5 – Basic Port Control Model for Transitioning a Port out of L1	757
Figure 4-6 – Host Initiated L1 to L0 Transition (L1 Exit)	757
Figure 4-7 – USB 2.0 Hub Reference Port State Machine Relationships with L1 Additions	758
Figure 4-8 – L1 Addendum to the Upstream Facing Port Receiver State Machine	759
Figure 4-9 – Addendum to the Upstream Facing Port Transmitter State Machine	761
Figure 4-10 – Addendum to the Internal Port State Machine	762
Figure 4-11 – Addendum to Downstream Facing Hub Port State Machine	764
Figure 7-29 – Connect Event Timing	786
Table 5-1 – Low-speed Control Transfer Limits	65
Table 5-2 – Full-speed Control Transfer Limits.....	66
Table 5-3 – High-speed Control Transfer Limits	66
Table 5-4 – Full-speed Isochronous Transaction Limits	68
Table 5-5 – High-speed Isochronous Transaction Limits	69
Table 5-6 – Low-speed Interrupt Transaction Limits	72
Table 5-7 – Full-speed Interrupt Transaction Limits	72

Table 5-8 – High-speed Interrupt Transaction Limits	73
Table 5-9 – Full-speed Bulk Transaction Limits	76
Table 5-10 – High-speed Bulk Transaction Limits	76
Table 5-11 – <i>wMaxPacketSize</i> Field of Endpoint Descriptor	77
Table 5-12 – Synchronization Characteristics	92
Table 5-13 – Connection Requirements	98
Table 6-1 – USB Connector Termination Assignment	112
Table 6-2 – Power Pair	120
Table 6-3 – Signal Pair	120
Table 6-4 – Drain Wire Signal Pair	121
Table 6-5 – Nominal Cable Diameter	122
Table 6-6 – Conductor Resistance	122
Table 6-7 – USB Electrical, Mechanical, and Environmental Compliance Standards	123
Table 6-7 – USB Electrical, Mechanical, and Environmental Compliance Standards (Continued)	124
Table 7-1 – Description of Functional Elements in the Example Shown in Figure 7-1	134
Table 7-2 – Low-/full-speed Signaling Levels	157
Table 7-3 – High-speed Signaling Levels	160
Table 7-3 – High-speed Signaling Levels (Continued)	161
Table 7-4 – Full-speed Jitter Budget	178
Table 7-5 – Low-speed Jitter Budget	179
Table 7-6 – Maximum Allowable Cable Loss	181
Table 7-7 – DC Electrical Characteristics	192
Table 7-7 – DC Electrical Characteristics (Continued)	193
Table 7-7 – DC Electrical Characteristics (Continued)	194
Table 7-8 – High-speed Source Electrical Characteristics	194
Table 7-9 – Full-speed Source Electrical Characteristics	195
Table 7-10 – Low-speed Source Electrical Characteristics	196
Table 7-11 – Hub/Repeater Electrical Characteristics	197
Table 7-12 – Cable Characteristics (Note 14)	198
Table 7-13 – Hub Event Timings	199
Table 7-13 – Hub Event Timings (Continued)	200
Table 7-14 – Device Event Timings	200
Table 7-14 – Device Event Timings (Continued)	201
Table 8-1 – PID Types	206
Table 8-2 – Isochronous OUT Payload Continuation Encoding	213
Table 8-3 – Endpoint Type Values in Split Special Token	214
Table 8-4 – Function Responses to IN Transactions	217
Table 8-5 – Host Responses to IN Transactions	218
Table 8-6 – Function Responses to OUT Transactions in Order of Precedence	218
Table 8-7 – Status Stage Responses	237
Table 8-8 – Packet Error Types	247
Table 9-1 – Visible Device States	252

Table 9-2 – Format of Setup Data	259
Table 9-3 – Standard Device Requests	261
Table 9-4 – Standard Request Codes	261
Table 9-5 – Descriptor Types	262
Table 9-6 – Standard Feature Selectors	262
Table 9-7 – Test Mode Selectors	268
Table 9-8 – Standard Device Descriptor	271
Table 9-9 – Device _ Qualifier Descriptor	273
Table 9-10 – Standard Configuration Descriptor	274
Table 9-11 – Other_Speed_Configuration Descriptor	275
Table 9-12 – Standard Interface Descriptor	276
Table 9-13 – Standard Endpoint Descriptor	277
Table 9-13 – Standard Endpoint Descriptor (<i>Continued</i>)	278
Table 9-14 – Allowed wMaxPacketSize Values for Different Numbers of Transactions per Microframe	279
Table 9-15 – String Descriptor Zero, Specifying Languages Supported by the Device	280
Table 9-16 – UNICODE String Descriptor	280
Table 11-1 – High-speed Microframe Timer Range Contributions	306
Table 11-2 – Full-speed Frame Timer Range Contributions	307
Table 11-3 – Hub and Host EOF1/EOF2 Timing Points	309
Table 11-4 – Internal Port Signal/Event Definitions	314
Table 11-5 – Downstream Facing Port Signal/Event Definitions	317
Table 11-6 – Automatic Port State to Port Indicator Color Mapping	323
Table 11-7 – Port Indicator Color Definitions	324
Table 11-8 – Upstream Facing Port Receiver Signal/Event Definitions	326
Table 11-9 – Upstream Facing Port Transmit Signal/Event Definitions	329
Table 11-10 – High-speed Port Selector Signal/Event Definitions	332
Table 11-11 – Hub Repeater Signal/Event Definitions	333
Table 11-12 – Hub Power Operating Mode Summary	346
Table 11-13 – Hub Descriptor	419
Table 11-14 – Hub Responses to Standard Device Requests	420
Table 11-15 – Hub Class Requests	421
Table 11-16 – Hub Class Request Codes	422
Table 11-17 – Hub Class Feature Selectors	422
Table 11-18 – wValue Field for Clear_TT_Buffer	424
Table 11-19 – Hub Status Field, wHubStatus	425
Table 11-20 – Hub Change Field, wHubChange	426
Table 11-21 – Port Status Field, wPortStatus	427
Table 11-22 – Port Change Field, wPortChange	431
Table 11-23 – Format of Returned TT State	432
Table 11-24 – Test Mode Selector Codes	436
Table 11-25 – Port Indicator Selector Codes	436
Table 5-3 – High-speed Control Transfer Limits	636

Table 5-8 – High-speed Interrupt Transaction Limits	637
Table 5-5 – High-speed Isochronous Transaction Limits	638
Table 9-3 – Standard Device Requests	647
Table 11-14 – Hub Responses to Standard Device Requests.....	663
Table 11-21 – Port Status Field, wPortStatus.....	665
Table 6-1 – USB Series “A” and Series “B” Connector Termination Assignment.....	682
Table 6-2 – USB Series “mini-B” Connector Termination Assignment.....	682
Table 6-26-3 – Power Pair	695
Table 6-36-4 – Signal Pair	695
Table 6-46-5 – Drain Wire Signal Pair	696
Table 6-56-6 – Nominal Cable Diameter	697
Table 6-66-7 – Conductor Resistance	697
Table 6-76-8 – USB Electrical, Mechanical, and Environmental Compliance Standards	698
Table 6-76-8 – USB Electrical, Mechanical, and Environmental Compliance Standards (Continued).....	699
Table 6-76-8 – USB Electrical, Mechanical, and Environmental Compliance Standards (Continued).....	700
Table 6-76-8 – USB Electrical, Mechanical, and Environmental Compliance Standards (Continued).....	701
Table 6-76-8 – USB Electrical, Mechanical, and Environmental Compliance Standards (Continued).....	702
Table 9-13 – Standard Endpoint Descriptor (Continued)	717
Table 11-6 – Automatic Port State to Port Indicator Color Mapping	719
Table 9-5 – Descriptor Types	733
Table 9-13 – Standard Interface Association Descriptor.....	734
Table 9-4314 – Standard Endpoint Descriptor.....	734
Table 9-16 – UNICODE String Descriptor	740
Table 1-1 – USB Link Power Management (Lx) States	743
Table 1-2 – Summary Similarities/Differences Between L1 and L2	744
Table 2-1 – PID Types	745
Table 2-2 – SubPID Types	747
Table 2-2 – SubPID Types (cont.)	747
Table 2-3 – LPM Token <i>bmAttributes</i> Field Definition.....	748
Table 3-1 – USB Device Capabilities – USB 2.0 Extension Descriptor	749
Table 3-1 – USB Device Capabilities – USB 2.0 Extension Descriptor (cont.).....	750
Table 4-1 – Device Initiated Resume Propagation and Adjacent Port Side-effects	756
Table 4-2 – Upstream Facing Port Receiver Signal/Event Definitions (Addendum).....	759
Table 4-3 – Upstream Facing Port Transmitter Signal/Event Definitions (Addendum).....	761
Table 4-4 – Internal Port Signal/Event Definitions (Addendum)	763
Table 4-5 – Downstream Port Signal/Event Definitions (Addendum).....	764
Table 4-6 – Summary LPM Timing Characteristics	767
Table 4-7 – Hub Class Feature Selectors.....	767
Table 4-7 – Hub Class Feature Selectors (cont.).....	768
Table 4-8 – <i>wIndex</i> Definition for Clear Port Feature on an LPM Enabled Hub	768

Table 4-9 – Port Status Bits with L1 Additions.....	769
Table 4-10 – Port Change Bits with L1 Additions.....	770
Table 4-11 – Set and Test Port Feature Details	771
Table 9-7. Test Mode Selectors	787
Table 9-7. Test Mode Selectors	787

NOTE All Engineering Change Notice's (ECN) and Errata documents as of September 01, 2012 that pertain to this core specification follow the last page of the specification starting on page 635.

Universal Serial Bus Specification

Compaq
Hewlett-Packard
Intel
Lucent
Microsoft
NEC
Philips

Revision 2.0
April 27, 2000

Scope of this Revision

The 2.0 revision of the specification is intended for product design. Every attempt has been made to ensure a consistent and implementable specification. Implementations should ensure compliance with this revision.

Revision History

Revision	Issue Date	Comments
0.7	November 11, 1994	Supersedes 0.6e.
0.8	December 30, 1994	Revisions to Chapters 3-8, 10, and 11. Added appendixes.
0.9	April 13, 1995	Revisions to all the chapters.
0.99	August 25, 1995	Revisions to all the chapters.
1.0 FDR	November 13, 1995	Revisions to Chapters 1, 2, 5-11.
1.0	January 15, 1996	Edits to Chapters 5, 6, 7, 8, 9, 10, and 11 for consistency...
1.1	September 23, 1998	Updates to all chapters to fix problems identified.
2.0 (draft 0.79)	October 5, 1999	Revisions to chapters 5, 7, 8, 9, 11 to add high speed.
2.0 (draft 0.9)	December 21, 1999	Revisions to all chapters to add high speed.
2.0	April 27, 2000	Revisions for high-speed mode.

Universal Serial Bus Specification
Copyright © 2000, Compaq Computer Corporation,
Hewlett-Packard Company,
Intel Corporation,
Lucent Technologies Inc,
Microsoft Corporation,
NEC Corporation,
Koninklijke Philips Electronics N.V.
All rights reserved.