

Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 2-719: Test methods for materials for interconnection structures - Relative permittivity and loss tangent (500 MHz to 10 GHz)

## EESTI STANDARDI EESSÕNA

## NATIONAL FOREWORD

See Eesti standard EVS-EN 61189-2-719:2016 sisaldab Euroopa standardi EN 61189-2-719:2016 ingliskeelset teksti.	This Estonian standard EVS-EN 61189-2-719:2016 consists of the English text of the European standard EN 61189-2-719:2016.
Standard on jõustunud sellekohase teate avaldamisega EVS Teatajas	This standard has been endorsed with a notification published in the official bulletin of the Estonian Centre for Standardisation.
Euroopa standardimisorganisatsioonid on teinud Euroopa standardi rahvuslikele liikmetele kättesaadavaks 14.10.2016.	Date of Availability of the European standard is 14.10.2016.
Standard on kättesaadav Eesti Standardikeskusest.	The standard is available from the Estonian Centre for Standardisation.

Tagasisidet standardi sisu kohta on võimalik edastada, kasutades EVS-i veebilehel asuvat tagasiside vormi või saates e-kirja meiliaadressile [standardiosakond@evs.ee](mailto:standardiosakond@evs.ee).

ICS 31.180

Standardite reprodutseerimise ja levitamise õigus kuulub Eesti Standardikeskusele

Andmete paljundamine, taastekitamine, kopeerimine, salvestamine elektroonsesse süsteemi või edastamine ükskõik millises vormis või millisel teel ilma Eesti Standardikeskuse kirjaliku loata on keelatud.

Kui Teil on küsimusi standardite autorikaitse kohta, võtke palun ühendust Eesti Standardikeskusega:

Aru 10, 10317 Tallinn, Eesti; koduleht [www.evs.ee](http://www.evs.ee); telefon 605 5050; e-post [info@evs.ee](mailto:info@evs.ee)

The right to reproduce and distribute standards belongs to the Estonian Centre for Standardisation

No part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying, without a written permission from the Estonian Centre for Standardisation.

If you have any questions about copyright, please contact Estonian Centre for Standardisation:

Aru 10, 10317 Tallinn, Estonia; homepage [www.evs.ee](http://www.evs.ee); phone +372 605 5050; e-mail [info@evs.ee](mailto:info@evs.ee)

ICS 31.180

English Version

Test methods for electrical materials, printed boards and other  
interconnection structures and assemblies -  
Part 2-719: Test methods for materials for interconnection  
structures - Relative permittivity and loss tangent (500 MHz to 10  
GHz)  
(IEC 61189-2-719:2016)

Méthode d'essai pour les matériaux électriques, les cartes  
imprimées et autres structures d'interconnexion et  
ensembles - Partie 2-719: Méthodes d'essai des matériaux  
pour structures d'interconnexion - Permittivité relative et  
tangente de perte (500 MHz à 10 GHz)  
(IEC 61189-2-719:2016)

Prüfverfahren für Elektromaterialien, Leiterplatten und  
andere Verbindungsstrukturen und Baugruppen -  
Teil 2-719: Prüfverfahren für Materialien von  
Verbindungsstrukturen - Relative Permittivität und  
Verlustfaktor (500 MHz bis 10 GHz)  
(IEC 61189-2-719:2016)

This European Standard was approved by CENELEC on 2016-08-16. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the CEN-CENELEC Management Centre or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CEN-CENELEC Management Centre has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.



European Committee for Electrotechnical Standardization  
Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

CEN-CENELEC Management Centre: Avenue Marnix 17, B-1000 Brussels

## European foreword

The text of document 91/1366/FDIS, future edition 1 of IEC 61189-2-719, prepared by IEC/TC 91 "Electronics assembly technology" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 61189-2-719:2016.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2017-05-16
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2019-08-16

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

## Endorsement notice

The text of the International Standard IEC 61189-2-719:2016 was approved by CENELEC as a European Standard without any modification.

## Annex ZA (normative)

### Normative references to international publications with their corresponding European publications

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE 1 When an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

NOTE 2 Up-to-date information on the latest versions of the European Standards listed in this annex is available here: [www.cenelec.eu](http://www.cenelec.eu)

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60194	-	Printed board design, manufacture and assembly - Terms and definitions	-	-

## CONTENTS

FOREWORD.....	4
1 Scope.....	6
2 Normative references .....	6
3 Terms and definitions .....	6
4 Test methods.....	6
4.1 Test specimens.....	6
4.1.1 General .....	6
4.1.2 Size .....	6
4.1.3 Thickness of dielectric.....	6
4.1.4 Thickness of copper foil .....	6
4.2 Test set .....	7
4.3 Test fixture.....	9
4.4 Test equipment .....	11
4.5 Procedure .....	11
4.5.1 Measurements .....	11
4.5.2 Calculations.....	12
5 Report.....	14
6 Additional information .....	14
6.1 Accuracy.....	14
6.2 Additional information concerning fixtures and results .....	14
Annex A (informative) Example of test fixture and test results .....	15
A.1 Dimension example of a test fixture .....	15
A.2 Example of test results .....	19
Figure 1 – One side of board A .....	7
Figure 2 – Another side of board A.....	7
Figure 3 – Cross section between X1 and X2 of board A.....	8
Figure 4 – Cross section between Y1 and Y2 of board A.....	8
Figure 5 – One side of board B .....	8
Figure 6 – Another side of board B.....	9
Figure 7 – Cross-section between X1 and X2 of board B.....	9
Figure 8 – Cross section between Y1 and Y2 of board B.....	9
Figure 9 – Top view of test fixture .....	10
Figure 10 – Horizontal cross section of test fixture with test set .....	10
Figure 11 – Side view of test fixture .....	10
Figure 12 – Vertical cross-section of test fixture with test set .....	11
Figure 13 – Example of VNA raw data .....	12
Figure 14 – Envelopes of raw data from VNA measurement .....	14
Figure A.1 – Parts of test fixture.....	17
Figure A.2 – Construction of parts .....	18
Figure A.3 – Part for connector attachment .....	18
Figure A.4 – Attachment with connector .....	19
Figure A.5 – An example of measured $\epsilon_r$ data, PTFE CCL .....	19

Figure A.6 – An example of measured  $\tan \delta$  data, PTFE CCL.....20

This document is a preview generated by EVS