IEC 63003

Edition 1.0 2015-12

INTERNATIONAL STANDARD

IEEE Std 1505.1™

colour inside

Standard for the common test interface pin map configuration for high-density, single-tier electronics test requirements utilizing IEEE Std 1505™

IEC 63003:2015-12(en) IEEE Std 1505.1-2008

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 25.040

ISBN 978-2-8322-2941-5

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STANDARD FOR THE COMMON TEST INTERFACE PIN MAP CONFIGURATION FOR HIGH-DENSITY, SINGLE-TIER ELECTRONICS TEST REQUIREMENTS UTILIZING IEEE Std 1505™

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The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
IEEE Std 1505.1-2008	91/1274/FDIS	91/1298/RVD

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IEEE Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™

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IEEE Standards Coordinating Committee 20 on Test and Diagnosis for Electronic Systems

Approved 26 September 2008

IEEE-SA Standards Board

Approved as a Full-Use Standard on 14 June 2013

IEEE-SA Standards Board

Abstract: This standard represents an extension to the IEEE 1505 receiver fixture interface (RFI) standard specification. Particular emphasis is placed on defining within the IEEE 1505 RFI standard a more specific set of performance requirements that employ a common scalable: (a) pin map configuration; (b) specific connector modules; (c) respective contacts; (d) recommended switching implementation; and (e) legacy automatic test equipment (ATE) transitional devices. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future automatic test systems (ATS).

Keywords: ATE, ATS, fixture, ICD, IEEE 1505.1™, interface, ITA, mass termination, receiver, scalable, TPS, UUT

IEEE Introduction

This introduction is not part of IEEE Std 1505.1-2008, IEEE Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™.

This standard stems from the history of ATE implementations having unique input/output (I/O) pin out definitions. This uniqueness has prevented the interoperability of test program sets (TPSs) among different ATEs within the same organizations. Even if the same RFI was used by the target ATE, the signals I/O could not be guaranteed to be at the same pin location. This is due to there being no suitable standard pin out definition for general purpose electronic testing applications.

IEEE Std 1505-2006[a] has addressed part of the interoperability problem by defining the common mechanical interface for the ATE. This project takes the TPS interoperability problem one step further toward completion by standardizing the electrical signal I/O pin map for general purpose electronic testing applications.

Particular emphasis is placed on defining within the IEEE 1505 RFI standard a more specific set of performance requirements that employ a common scalable: (a) framework; (b) pin map configuration; (c) specific connector modules; (d) respective contacts; (e) recommended switching implementation; and (f) legacy ATE transitional devices. This is intentionally done to standardize the footprint and assure mechanical and electrical interoperability between past and future ATS. The suggested mechanical and electrical requirements necessary to implement a specific IEEE 1505 RFI product in support of a common test interface (CTI) across all U.S. Department of Defense (DoD) defense agencies, related aerospace industry, and a variety of non-U.S. government agencies such as the U.K. Ministry of Defense (MoD) is provided.

The DoD is a major buyer and user of ATE; however, existing acquisition guidance desires the use of commercial standards and/or best practices for these systems. Suitable standards currently do not exist in the commercial marketplace; therefore, this standard will provide such specification.

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[a] Information on references can be found in Clause 2.

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Standard for the Common Test Interface Pin Map Configuration for High-Density, Single-Tier Electronics Test Requirements Utilizing IEEE Std 1505™

1. Overview

1.1 Scope

The scope of this standard is the definition of a pin map utilizing the IEEE 1505™ [1] receiver fixture interface (RFI). The pin map defined within this standard shall apply to military and aerospace automatic test equipment (ATE) testing applications.

[1] Information on references can be found in Clause 2.

1.2 Purpose

Standardization of a common input/output (I/O) will enable the interoperability of IEEE 1505 compliant interface fixtures [also known as *interface test adapters* (ITA), *interface devices* (IDs), or *interconnecting devices* (ICDs)] on multiple ATE systems utilizing the IEEE 1505 RFI.

1.3 Statement of the problem

1.3.1 U.S. Government guidance

From 1980 to 1992, the U.S. Department of Defense (DoD) investment in field, depot, and factory automatic test systems (ATS) exceeded $35 billion with an additional $15 billion for associated support. Most of this test capability was acquired as part of individual weapon system procurements. This led to a proliferation of different custom equipment types with unique interfaces. Recent policy decisions have changed the direction of the purchase of test equipment towards a standards based approach with both hardware and software critical interface requirements.

The U.S. DoD Instruction 5000.2-R1 ATS Policy states: "ATS capabilities shall be defined through critical hardware and software elements" (see [B2][2]). This policy however, did not define these critical elements. The Critical Interfaces Project was created to define critical ATS elements.

1.3.2 Critical Interfaces Project

The Factory-to-Field Integration of Defense Test Systems Project (commonly referred to as the *Critical Interfaces Project*) was started in the latter part of 1995. The Critical Interfaces Working Group (CIWG) within the Joint-Service ATS Research and Development Integrated Product Team (ARI) was established to perform the project. The ATS Executive Agent Office (EAO) has provided project management and coordination among the Air Force, Army, Marine Corps, and Navy participants. In addition, many industry representatives have participated. The CIWG published their findings in the Automatic Test System Critical Interfaces Report [B1] and this report served as the basis for the development of the RFI architecture and subsequent specification.

The objective of the Critical Interfaces Project was to demonstrate the feasibility of reducing the cost to re-host test program sets (TPSs) and increase the interoperability of TPS software among the military services by using standardized interfaces.

Interfaces that offer the potential to achieve this objective are deemed critical. Potential savings will be quantified through demonstration. The Automatic Test System Critical Interfaces Report [B1] is maintained by the ATS EAO and provides guidance to DoD ATE acquisition programs. This document also addressed the requirements of DoD Regulation 5000.2-R1 [B2] and assisted in migrating the DoD designated tester families towards a common solution. The Hardware Interfaces (HI) Subcommittee of the IEEE Standards Coordinating Committee on Test and Diagnosis for Electronic Systems (SCC20) applied the recommendations of the report as it related to the RFI, to the extent that the current RFI standard is in full compliance with the report.

1.3.3 CTIWG guidance recommendations

During the Common Test Interface Working Group (CTIWG) October 2003 meeting, the DoD provided the following recommendations as guidance for the Working Group's success:

[2] The numbers in brackets correspond to those of the bibliography in Annex B.

a) Identify a modular/scaleable interface
b) Allow use of different size ID/fixture on the same general purpose interface (GPI)
c) Ensure TPS hardware compatibility as interface grows
d) Provide legacy system support
e) Provide a transition path to support legacy TPS hardware
f) Adhere to an open architecture system
g) Built to one specification
h) Multiple sources
i) Non-proprietary design and components
j) Ensure capabilities that provision for growth and special requirements
k) Provide room for future expansion and TPS requirements
l) Support and Promote the use of commercial-off-the-shelf (COTS) interconnect components
m) Use industry standard connector technology

1.3.4 CTIWG legacy test program set support

In support of these recommendations, the CTI architecture shall assure past legacy and future TPS *plug and play* compatibility between defense agencies and defense-aerospace suppliers. Areas addressed by the CTIWG include:

a) Pin mapping
b) Scalability
c) TPS legacy support
d) Connector parametric (dc to light)
e) Reliability and maintainability
f) Physical
g) Switching
h) Design-to-cost factors

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated referenced, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1505-2006, IEEE Standard for Receiver Fixture Interface.[3, 4]

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