Semiconductor devices - Mechanical and climatic test methods - Part 15: Resistance to soldering temperature for through-hole mounted devices



## EESTI STANDARDI EESSÕNA

## NATIONAL FOREWORD

| Käesolev Eesti standard EVS-EN 60749-  | This Estonian standard EVS-EN 60749-15:2010   |  |  |  |
|--|---|--|--|--|
| 15:2010 sisaldab Euroopa standardi EN 60749-<br>15:2010 ingliskeelset teksti.          | consists of the English text of the European standard EN 60749-15:2010.                             |  |  |  |
|  | Standard EN 60749-15.2010.  |  |  |  |
| Standard on kinnitatud Eesti Standardikeskuse  | This standard is ratified with the order of   |  |  |  |
| 31.12.2010 käskkirjaga ja jõustub sellekohase  | Estonian Centre for Standardisation dated   |  |  |  |
| teate avaldamisel EVS Teatajas.  | 31.12.2010 and is endorsed with the notification published in the official bulletin of the Estonian |  |  |  |
| 5.   | national standardisation organisation.  |  |  |  |
| U.S.   |   |  |  |  |
| Euroopa standardimisorganisatsioonide poolt  | Date of Availability of the European standard text  |  |  |  |
| rahvuslikele liikmetele Euroopa standardi teksti<br>kättesaadavaks tegemise kuopäev on | 10.12.2010.   |  |  |  |
| 10.12.2010.  |   |  |  |  |
| 3  |   |  |  |  |
| Standard on kättesaadav Eesti  | The standard is available from Estonian   |  |  |  |
| standardiorganisatsioonist.  | standardisation organisation.   |  |  |  |
|  | 10.12.2010.<br>The standard is available from Estonian<br>standardisation organisation.             |  |  |  |
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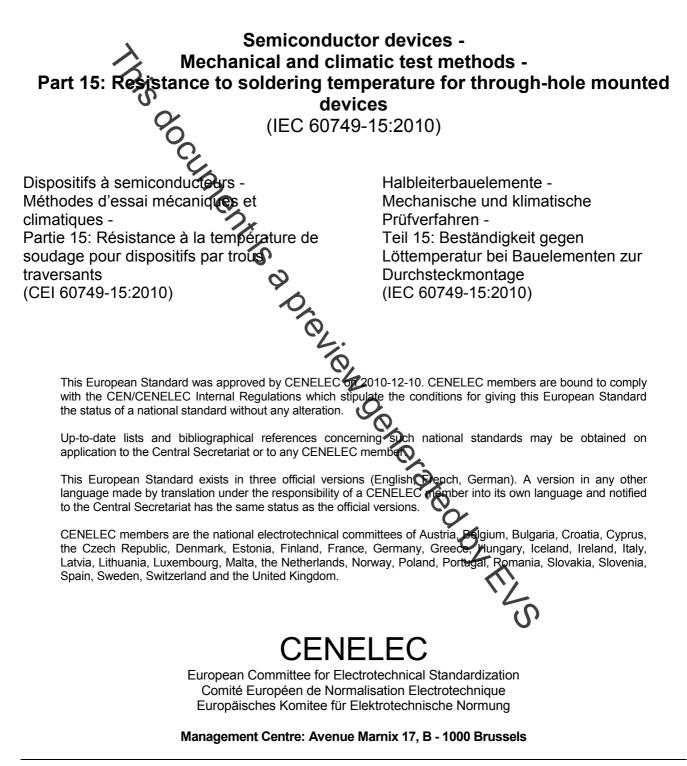
# EN 60749-15

December 2010

ICS 31.080.01

Supersedes EN 60749-15:2003

English version



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## Foreword

The text of document 47/2067/FDIS, future edition 2 of IEC 60749-15, prepared by IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60749-15 on 2010-12-01.

This European Standard supersedes EN 60749-15:2003.

The significant changes with respect from EN 60749-15:2003 include:

- editorial change in the scope,
- addition of lead free solder chemical composition specification.

Attention is drawn the possibility that some of the elements of this document may be the subject of patent rights. CEN and CENELEC shall not be held responsible for identifying any or all such patent rights.

The following dates were f

| _ | latest date by which the EN has to be implemented       |       |            |
|---|---|-------|------------|
|   | at national level by publication an identical           |       |            |
|   | national standard or by endorsement                     | (dop) | 2011-09-01 |
|   |   |       |            |
|   | latest data by which the national standards conflicting |       |            |

latest date by which the national standards conflicting with the EN have to be withdrawn

Annex ZA has been added by CENELEC

Endorsement notice

2013-12-01

(dow)

The text of the International Standard IEC 60749-15:2010 was approved by CENELEC as a European Standard without any modification.

De later ou trues  $\mathbf{\Omega}$ In the official version, for Bibliography, the following note has to be added for the standard indicated:

IEC 60068-2-20 NOTE Harmonized as EN 60068-2-20.

## SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

# Part 15: Resistance to soldering temperature for through-hole mounted devices

## 1 Scope 🍃

This part of IEC 60749 describes a test used to determine whether encapsulated solid state devices used for through-hole mounting can withstand the effects of the temperature to which they are subjected during soldering of their leads by using wave soldering or a soldering iron.

In order to establish a standard test procedure for the most reproducible methods, the solder dip method is used because of its more controllable conditions. This procedure determines whether devices are capable of withstanding the soldering temperature encountered in printed wiring board assembly operations, without degrading their electrical characteristics or internal connections.

This test is destructive and may be described for qualification, lot acceptance and as a product monitor.

This test is, in general, in conformity with UEC 60068-2-20 but, due to specific requirements of semiconductors, the clauses of this standard apply.

## 2 General

The heat is conducted through the leads into the revice package from solder heat at the reverse side of the board. This procedure does not simulate wave soldering or reflow heat exposure on the same side of the board as the package body.

## 3 Test apparatus

#### 3.1 Solder pot

A solder pot of sufficient size to contain at least 1 kg of solder shape used. The solder pot dimensions shall allow full immersion of the leads without touching the bottom. The apparatus shall be capable of maintaining the solder at the temperature specified in table 1.

#### 3.2 Dipping device

A mechanical dipping device shall be used that is capable of controlling the rates of immersion and emersion of the leads and providing the dwell time as specified in Table 1.

#### 3.3 Heatsinks or shielding

If applicable, heatsinks or shielding shall be attached to the devices prior to the test and shall be as specified in the relevant specification.