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Guidelines for representing switching losses of SIC MOSFETs in datasheets

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It is based upon JEDEC JEP187: *Guidelines for Representing Switching Losses of SiC MOSFETs in Datasheets*. It is used with permission of the copyright holder, JEDEC Solid State Technology Association. It was submitted as a Fast Track document.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2987/FDIS	47/2995/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

This document was developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

– reconfirmed,
– withdrawn, or
– revised.

INTRODUCTION

This document is intended for use in the SiC power semiconductor and related power electronic industries and provides guidelines for representation of switching losses and related measurement conditions on SiC MOSFET device datasheets.

Switching losses are key parameters for evaluating power device performance, for benchmarking devices of different manufacturers and deciding on the suitability of a device in an application. Measurement and/or setup parameters can have a significant influence on the measured switching losses. Without clear definition of the methodology used, it is not possible to compare devices properly or, in some cases, even decide on its suitability for the target purpose.

The purpose of this document is to point out the factors that can influence switching losses for silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) and provide guidelines for a clean representation in datasheets.

1 Scope

This document specifies how to correctly display essential parameters of SiC-based PECS devices having a gate dielectric region biased to turn devices on and off. This typically refers to MOS devices such as MOSFETs and IGBTs. In this document, only NMOS devices are discussed as these are dominant for power device applications; however, the procedures apply to PMOS devices as well. In contrast to silicon power MOSFETs certain aspects of SiC power MOSFETs require a dedicated approach in order to represent device parameters correctly in the datasheet. Details are explained in the following paragraphs, among others the most important topics are:

– substantially higher switching speeds ad high V_{DS};

– strong impact of test setup (see Clause 5);

– impact of body diode as a function of the applied negative gate bias ant the limitations arising for the $V_{G(off)}$ values depending on the actual device.

This document does not define device failure criteria, acceptable use conditions or acceptable lifetime targets. That is up to the device manufacturers and users. However, it provides stress procedures such that the threshold voltage stability over time as affected by gate bias and temperature can be demonstrated and evaluated.

2 Normative references

There are no normative references in this document.

3 Terms, definitions and letter symbols

3.1 Terms and definitions

No terms and definitions are listed in this document.

Symbols used in this document refer partially to definitions in IEC 60747-2 and IEC 60747-8.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

– IEC Electropedia: available at https://www.electropedia.org/

– ISO Online browsing platform: available at https://www.iso.org/obp

3.2 Letter symbols

The following letter symbols are used in this document:

DUT	Device Under Test
FWD	Free-wheeling diode
PECS	Power Electronic Conversion Semiconductor
E_{ON}	Turn-on switching energy losses
C_{GS}	Gate-source capacitance
C_{GD}	Gate-drain capacitance
C_{DS}	Drain-source capacitance
C_{ISS}	Input capacitance
C_{OSS}	Output capacitance
C_{RSS}	Reverse-transfer capacitance