Mechanical standardization of semiconductor devices - Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for stacked packages - Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array (P-PFBGA and P-PFLGA)

EESTI STANDARDIKESKUS
ESTONIAN CENTRE FOR STANDARDISATION

EESTI STANDARDI EESSÕNA	NATIONAL FOREWORD
Käesolev Eesti standard EVS-EN 60191-6-17:2011 sisaldab Euroopa standardi EN 60191-6-17:2011 ingliskeelset teksti.	This Estonian standard EVS-EN 60191-6-17:2011 consists of the English text of the European standard EN 60191-6-17:2011.
Standard on kinnitatud Eesti Standardikeskuse 30.04.2011 käskkirjaga ja jõustub sellekohase teate avaldamisel EVS Teatajas.	This standard is ratified with the order of Estonian Centre for Standardisation dated 30.04.2011 and is endorsed with the notification published in the official bulletin of the Estonian national standardisation organisation.
Euroopa standardimisorganisatsioonide poolt rahvuslikele liikmetele Euroopa standardi teksti kättesaadavaks tegemise kuupäev on 15.04.2011.	Date of Availability of the European standard text 15.04.2011.
Standard on kättesaadav Eesti standardiorganisatsioonist.	The standard is available from Estonian standardisation organisation.

ICS 31.080.01

EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

EN 60191-6-17

April 2011

ICS 31.080.01

English version

Mechanical standardization of semiconductor devices - Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for stacked packages - Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

(IEC 60191-6-17:2011)

Normalisation mécanique des dispositifs à semiconducteurs -
Partie 6-17: Règles générales pour la préparation des dessins d'encombrement des dispositifs à semiconducteurs à montage en surface -
Guide de conception pour les boîtiers emplilés -
Boîtiers matriciels à billes et à pas fins et boîtiers matriciels à zone de contact plate et à pas fins (P-PFBGA et P-PFLGA)
(CEI 60191-6-17:2011)

Mechanische Normung von Halbleiterbauelementen -
Teil 6-17: Allgemeine Regeln für die Erstellung von Gehäusezeichnungen von SMD-Halbleitergehäusen -
Konstruktionsleitfaden für gestapelte Gehäuse -
Feinraster-Ball-Grid-Array und Feinraster-Land-Grid-Array (P-PFBGA/P-PFLGA)
(IEC 60191-6-17:2011)

This European Standard was approved by CENELEC on 2011-03-03. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, the Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland and the United Kingdom.

CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Management Centre: Avenue Marnix 17, B - 1000 Brussels

Ref. No. EN 60191-6-17:2011 E

Foreword

The text of document 47D/785/FDIS, future edition 1 of IEC 60191-6-17, prepared by SC 47D, Mechanical standardization for semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-17 on 2011-03-03.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN and CENELEC shall not be held responsible for identifying any or all such patent rights.

The following dates were fixed:

– latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2011-12-03
– latest date by which the national standards conflicting with the EN have to be withdrawn	(dow)	2014-03-03

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6-17:2011 was approved by CENELEC as a European Standard without any modification.

Annex ZA
(normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 60191-6	-	Mechanical standardization of semiconductor devices - Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages	EN 60191-6	-
IEC 60191-6-5	-	Mechanical standardization of semiconductor devices - Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine-pitch ball grid array (FBGA)	EN 60191-6-5	-

CONTENTS

INTRODUCTION

The trend toward downsizing and higher density of portable electronic devices has driven LSI packages into smaller and higher density configurations. The market demand of higher density has led to the development of the package stacking technology that enabled miniaturization and higher functionality. The objective of this design guide is to standardize outlines and to get interchangeability of individual stackable packages.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-17: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for stacked packages – Fine-pitch ball grid array and fine-pitch land grid array (P-PFBGA and P-PFLGA)

1 Scope

This part of IEC 60191 provides outline drawings and dimensions for stacked packages and individual stackable packages in the form of FBGA or FLGA.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document applies.

IEC 60191-6, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device package*

IEC 60191-6-5, *Mechanical standardization of semiconductor devices – Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages - Design guide for fine-pitch ball grid array (FBGA)*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60191-6 and the following apply.

3.1
individual stackable package
package with an array of metallic balls or lands on the underside of the package for the purpose of surface-mount on a printed circuit board and an array of footprints (lands) on the upper side of the package for stacking packages

NOTE The individual stackable cavity-up FLGA package is a part of this specification on the premise of stacking a cavity-down FBGA with cavity-up FLGA.

3.2
stacked package
assembly of multiple individual stackable packages in a stacked configuration

NOTE The top package can be a standard FBGA specified in IEC 60191-6-5 without any footprints on the upper side of the package. The stand-off height of this standard package, however, shall follow this design guide.

3.3
mould cap height (A_2)
height of the mould cap which contains wire-bonded die or of the exposed flip chip-bonded die with respect to the upper substrate surface of the package