

# INTERNATIONAL STANDARD

**IEC**  
**60191-6-6**

First edition  
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## **Mechanical standardization of semiconductor devices –**

### **Part 6-6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine pitch land grid array (FLGA)**

*Normalisation mécanique des dispositifs à semi-conducteurs –*

*Partie 6-6:  
Règles générales pour la préparation des dessins  
d'encombrement des dispositifs à semi-conducteurs  
pour montage en surface – Guide de conception  
des dispositifs FLGA*



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –**

**Part 6-6: General rules for the preparation of outline drawings  
of surface mounted semiconductor device packages –  
Design guide for fine-pitch land grid array (FLGA)**

FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work, International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 60191-6-6 has been prepared by subcommittee 47D: Mechanical standardization of semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47D/404/FDIS	47D/421/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2003. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this standard may be issued at a later date.

## INTRODUCTION

The demand for area array style packages exists because of the multi-functions and high performance of electrical equipment. The objective of this design guide is to standardize outlines and to get interchangeability of FLGA packages. The terminal pitch and package outlines of these fine-pitch array packages are smaller than those of LGA packages.

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## MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

### Part 6-6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch land grid array (FLGA)

#### 1 Scope

This part of IEC 60191 provides common outline drawings and dimensions for all types of structures and composed materials of fine-pitch land grid array (hereinafter called FLGA) whose terminal pitch is less than, or equal to, 0,80 mm and whose package body outline is square.

#### 2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60191. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60191 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60191 (all parts), *Mechanical standardization of semiconductor devices*

#### 3 Definitions

For the purposes of this part of IEC 60191, the following definitions, as well as those given in the other parts of this standard, apply.

##### 3.1

##### **flanged type**

type whose package body size (body length and width) consists of its own flange composed around the encapsulation or lid

##### 3.2

##### **type of real chip size**

type whose package body size (body length and width) consists of an encapsulation around the real chip only

##### 3.3

##### **FLGA**

packages with metal lands or metal bumps of which the terminal height is less than, or equal to, 100  $\mu\text{m}$ , and whose terminal pitch is less than, or equal to, 0,80 mm, positioned in an array on the base plane of the package as external terminals

This package structure makes it possible to surface-mount the packages to the printed circuit board